TECHNICAL MANUAL

FOR

KS-22424

T1D REPEATER AND FAULT LOCATING

TEST SET

Bowmar

Communica ions
Test
Equip.

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Acto  0172
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STABRO LABS

# TECHNICAL MANUAL

# FOR

# KS-22424

# T1D REPEATER AND FAULT LOCATING

# TEST SET

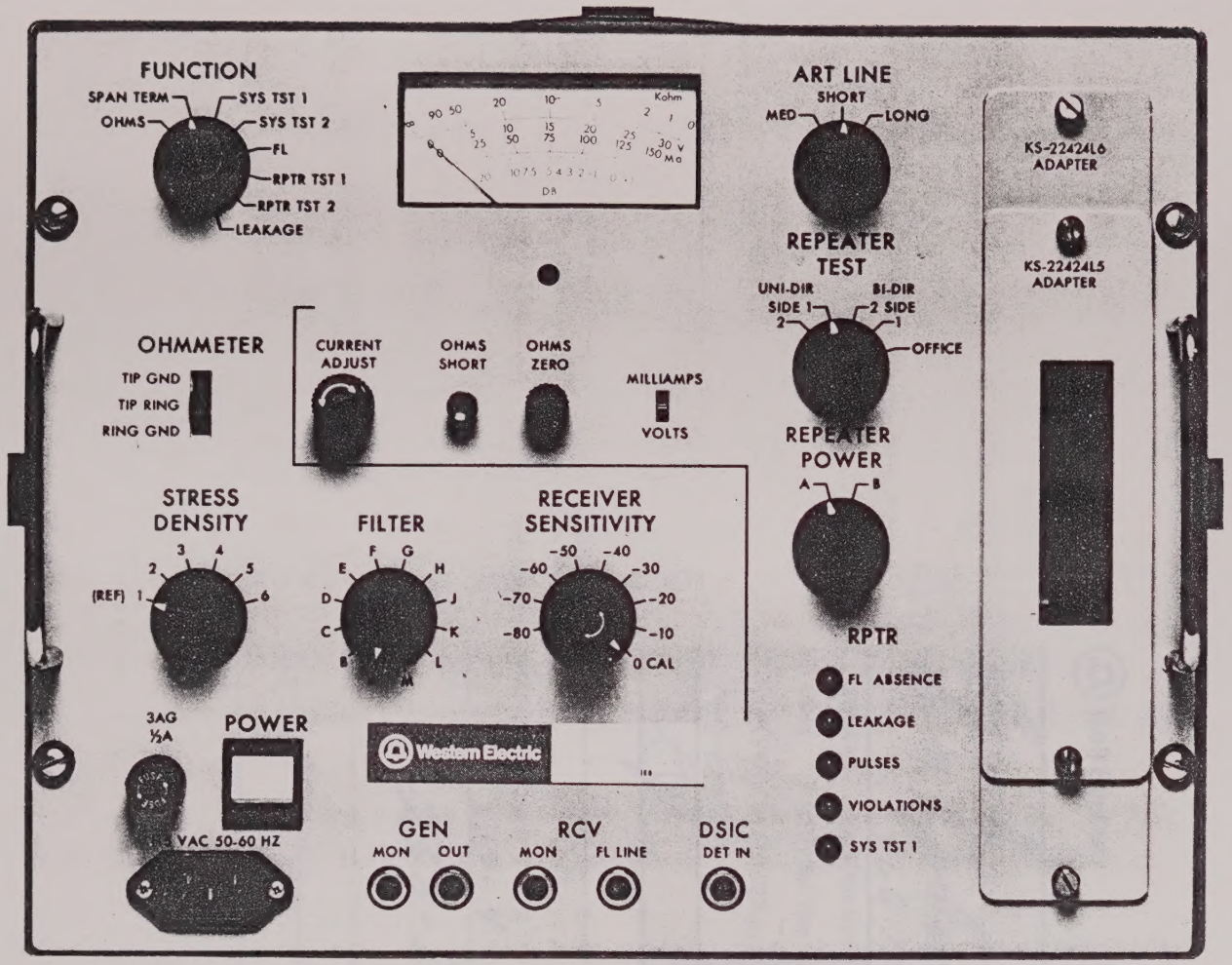
Manufactured For:

Western Electric Company

By

BOWMAR/ALI, INC.
531 Main Street
Acton, MA 01720

Revision 4
August, 1981


FUNCTION
SPAN TERM
OHMS
SYS TST 1
SYS TST 2
FL
RPTR TST 1
RPTR TST 2
LEAKAGE
Kohm
DB
ART LINE
SHORT
MED
LONG
KS-22424L6 ADAPTER
KS-22424L5 ADAPTER
REPEATER TEST
UNI-DIR
BI-DIR
SIDE 1
2 SIDE
2
1
OFFICE
OHMMETER
TIP GND
TIP RING
RING GND
CURRENT ADJUST
OHMS SHORT
OHMS ZERO
MILLIAMPS
VOLTS
REPEATER POWER
A
B
STRESS DENSITY
(REF)
FILTER
RECEIVER SENSITIVITY
0 CAL
RPTR
FL ABSENCE
LEAKAGE
PULSES
VIOLATIONS
SYS TST 1
3AG ½A
POWER
VAC 50-60 HZ
Western Electric
GEN
MON
OUT
RCV
MON
FL LINE
DSIC
DET IN

Bell System **Call Memo** BS-20 (10-80

To Leonard

From Ron Jackson

Tel. No. ( ) 766 1259 Ext.

| | | | |
|---|---|---|---|
| ☐ URGENT | ☐ Will Call Later | ☐ Job Ready | ☐ Contact |
| ☐ Called | ☐ To See You | ☐ Repro. | ☐ WP Ctr. |
| ☑ Please Call | ☐ Was Here | ☐ Graphics | ☐ Comm. Ctr. |
| ☐ Returned Your Call | | ☐ | |

Rec'd By LJ Date 1-11-82 Time 1535p

Call 4-5420
238-2394E

E-4940 (12-65)

# T CARRIER SYSTEM LAYOUT RECORD

BSP 365-000-01

| | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| A | CHANNEL GROUP: 217 Tie. ΦGDNUTMA · SLKCUTMA | | | | CONTROL OFFICE: NORTHERN SCC Toll | | | | |
| B | AREA MI.: 38.4 | AREA MI. | AREA MI. | TOTAL MI.: 38.4 | CKT. ORDER NO.: 10-6772-02 | DATE IN EFFECT | ISSUE NO.: 1 | CARD NO.: 2 OF 3 | |
| C | OFFICE A: ΦGDNUTMA | D TERM BAY: 1105.28 | BTA: D4A3 FR 13 | POSITION: 4A | OFFICE B: SLKCUTMA | D TERM BAY: 0100.14 | BTA: D4A3 FR 24 | POSITION: 1A | |

| D | TRANS. FROM A | | CASE SOCK. | SPAN TERM. ASSEMBLY INPUT | SPAN TERM. ASSEMBLY OUTPUT | OFFICE OR STATION | TRANS. FROM B | | CASE SOCK. | SPAN TERM ASSEMBLY INPUT | SPAN TERM ASSEMBLY OUTPUT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | CABLE | PAIR | | RR BAY NO POS | RR BAY NO POS | SPAN 6 SPAN | CABLE | PAIR | | RR BAY NO POS | RR BAY NO POS |
| | 1 | 2 | 3 | 4 | 5 | | 7 | 8 | 9 | 10 | 11 |
| E | | | | | | SCC System | | | | | |
| F | | | | | | | | | | | |
| G | | | | | | CARD 729 | | | | | |
| H | | | | | | | | | | | |
| I | | | | | | | | | | | |
| J | | | | | | | | | | | |
| K | SD1A210 | | | MAIN CGO | | | MAIN CGI | | | | |
| L | | | MT | 77.18-04 | | | MT 90.33-07 | | | | |
| M | | | MS | 07 2612 | | | MS 13 0515 | | | | |
| N | | | | FR-24 24 BIK A189 | | | FR-24 73 BIK B123 | | | | |
| O | | | | | | | | | | | |
| P | | | | CGA | | | CGA | | | | |
| Q | | | | 332 | | | 352 | | | | |
| R | | | | | | | | | | | |
| S | | | | | | | | | | | |
| T | | | | | | | | | | | |

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# ADDENDUM

On KS-22424 L1 Test Sets manufactured after October, 1981 and on earlier sets which have been updated, additional filters have been added to the Fault Locating Receiver Board (A5). A punch mark on the Test Set nameplate (after the serial number) indicates that the set has the latest filters. These filters change the board as follows:

| | | Part Numbers |
|---|---|---|
| C32A and C47 | 22 Microfarads | Mepco/Electra Part No. 3070CD220T040SF |
| C74 - Added in parallel with R9. + to +5V Supply | 33 Microfarads | Kemet Part No. T350F336M006AS |
| C72 - Added in parallel with R18. - to ground | 1 Microfarad | Kemet Part No. T350A105M035AS |
| C73 - Added in parallel with R53. - to ground | 1 Microfarad | Kemet Part No. T350A105M035AS |

TABLE OF CONTENTS


| | | Page |
|---|---|---|
| SECTION 1 | | |
| 1.0 | INTRODUCTION | 1-1 |
| 1.1 | Description | 1-1 |
| 1.2 | Scope | 1-3 |
| 1.3 | Summary Of Specifications | 1-3 |
| SECTION 2 | | |
| 2.0 | OPERATION | 2-1 |
| 2.1 | Controls, Indicators and Connectors | 2-1 |
| 2.2 | Operational Description | 2-3 |
| 2.2.1 | General | 2-3 |
| 2.2.2 | OHMS | 2-3 |
| 2.2.3 | SPAN TERM | 2-3 |
| 2.2.4 | SYS TST 1 | 2-4 |
| 2.2.5 | SYS TST 2 | 2-4 |
| 2.2.6 | FL | 2-4 |
| 2.2.7 | RPTR TST 1 | 2-6 |
| 2.2.8 | RPTR TST 2 | 2-9 |
| 2.2.9 | LEAKAGE | 2-9 |
| 2.2.10 | DS1C DET IN | 2-9 |
| 2.3 | Operating Instructions | 2-9 |
| 2.3.1 | General | 2-9 |
| 2.3.2 | Line Resistance Measurement | 2-9 |
| 2.3.3 | Line Noise Measurement | 2-11 |
| 2.3.4 | Fault Locating Tests | 2-11 |
| 2.3.5 | Repeater Testing (RTPR TST 1) | 2-12 |
| 2.3.6 | Repeater Testing (RPTR TST 2) | 2-12 |
| 2.3.7 | Line Repeater Leakage Testing | 2-13 |
| 2.3.8 | Other FUNCTION Switch Positions | 2-13 |
| 2.3.9 | Use of DS1C Receiver | 2-13 |
| 2.3.10 | Use of Monitor Jacks | 2-13 |
| SECTION 3 | | |
| 3.0 | THEORY OF OPERATION | 3-1 |
| 3.1 | Overview | 3-1 |
| 3.2 | A1 Transmitter Board (Schematic 5-3) | 3-1 |
| 3.3 | A4 Repeater Interface Board (Schematic 5-6) | 3-6 |
| 3.4 | A6 DET IN Receiver (Schematic 5-8) | 3-8 |
| 3.5 | A5 Fault Locating Receiver Board (Schematic 5-7) | 3-11 |
| 3.6 | A8 Power Supply Board (Schematic 5-10) | 3-15 |
| 3.7 | A7 Meter Board (Schematic 5-9) | 3-15 |
| 3.8 | A3 Converter Board (Schematic 5-5) | 3-15 |
| 3.9 | A2 Artificial Line Board (Schematic 5-4) | 3-16 |

TABLE OF CONTENTS (Con't)


| | | Page |
|---|---|---|
| SECTION 4 | | |
| 4.0 | MAINTENANCE | 4-1 |
| 4.1 | Test Equipment Requirements | 4-1 |
| 4.2 | Calibration | 4-3 |
| 4.3 | Performance Checks | 4-7 |
| SECTION 5 | DIAGRAMS | 5-1 |
| SECTION 6 | PARTS LISTS | 6-1 |

LIST OF FIGURES


| | | Page |
|---|---|---|
| Fig. 1-1: | Basic Fault Location Set Functional Block Diagram | 1-2 |
| Fig. 2-1: | Fault Locating Word Definition | 2-4 |
| Fig. 2-2: | Word Organization vs. Stress Level | 2-5 |
| Fig. 2-3: | Line Repeater Configurations | 2-6 |
| Fig. 2-4: | T1D Line Repeater Power Circuit | 2-7 |
| Fig. 2-5: | Typical Line Repeater Test Arrangement | 2-8 |
| Fig. 2-6: | Typical Office Repeater Test Arrangement | 2-10 |
| Fig. 3-1: | Line Repeater Testing Side One Selected RPTR TST 1 | 3-2 |
| Fig. 3-2: | Fault Locating Circuitry, Ohmmeter and Wideband Noise Circuitry | 3-3 |
| Fig. 3-3: | Transmitter Block Diagram | 3-4 |
| Fig. 3-4: | Repeater Interface Block Diagram | 3-7 |
| Fig. 3-5: | DET IN Block Diagram | 3-9 |
| Fig. 3-6: | Fault Locating Receiver | 3-12 |
| Fig. 3-7: | Quadrature Signal Generation | 3-13 |
| Fig. 4-1 | Special Connector | 4-2 |
| Fig. 4-2: | Plug 3 | 4-2 |
| Fig. 4-3: | Plug 4 | 4-2 |
| Fig. 4-4: | Plug 2 | 4-2 |
| Fig. 4-5: | Plug 1 | 4-2 |
| Fig. 4-6: | Clock Extractor Adjustment | 4-6 |
| Fig. 4-7: | Clock Extractor Phase Adjustment | 4-6 |
| Fig. 4-8: | Bipolar Waveform | 4-7 |
| Fig. 4-9: | Set Up For SPAN TERM Testing | 4-9 |
| Fig. 4-10: | Fault Locate Test Arrangement | 4-11 |
| Fig. 5-1: | T1D Interconnect Schematic (Sheet 1) - T1D-110 | 5-2 |
| Fig. 5-2: | T1D Interconnect Schematic (Sheet 2) - T1D-110 | 5-3 |
| Fig. 5-3: | Transmitter Board (A1) Schematic - T1D-102 | 5-4 |
| Fig. 5-4: | Artificial Line Board (A2) Schematic - T1D-105 | 5-5 |
| Fig. 5-5: | T1C/T1D T1D/T1C Converter Board (A3) Schematic - T1D-106 | 5-6 |
| Fig. 5-6: | Repeater Interface Board (A4) Schematic - T1D-102 | 5-7 |
| Fig. 5-7: | Fault Locating Receiver (A5) Schematic - T1D-101 | 5-8 |
| Fig. 5-8: | DET IN Receiver (A6) Schematic - T1D-104 | 5-9 |
| Fig. 5-9: | Meter Interface Board (A7) Schematic - T1D-107 | 5-10 |
| Fig. 5-10: | Power Supply (A8) Schematic - T1D-109 | 5-11 |
| Fig. 5-11: | Transmitter Board (A1) Assembly Drawing - T1D-203 | 5-12 |
| Fig. 5-12: | Artificial Line Board (A2) Assembly Drawing - T1D-205 | 5-13 |

LIST OF FIGURES (Con't)


| | | Page |
|---|---|---|
| Fig. 5-13: | T1C/T1D T1D/T1C Converter Board (A3) Assembly Drawing - T1D-206 | 5-14 |
| Fig. 5-14: | Repeater Interface Board (A4) Assembly Drawing - T1D-202 | 5-15 |
| Fig. 5-15: | Fault Locating Receiver (A5) Assembly Drawing - T1D-201 | 5-16 |
| Fig. 5-16: | DET IN Receiver (A6) Assembly Drawing - T1D-204 | 5-17 |
| Fig. 5-17: | Meter Interface Board (A7) Assembly Drawing - T1D-207 | 5-18 |
| Fig. 5-18: | Power Supply Board (A8) Assembly Drawing - T1D-209 | 5-19 |
| Fig. 5-19: | Transmitter Board (A1) Circuit Pattern (Component Side) - PMT1D-403 | 5-20 |
| Fig. 5-20: | Transmitter Board (A1) Circuit Pattern (Non-Component Side) - PMT1D-403 | 5-21 |
| Fig. 5-21: | Artificial Line Board (A2) Circuit Pattern (Non-Component Side) - PMT1D-405 | 5-22 |
| Fig. 5-22: | T1C/T1D T1D/T1C Converter Board (A3) Circuit Pattern (Component Side) - PMT1D-406 | 5-23 |
| Fig. 5-23: | T1C/T1D T1D/T1C Converter Board (A3) Circuit Pattern (Non-Component Side) - PMT1D-406 | 5-24 |
| Fig. 5-24: | Repeater Interface Board (A4) Circuit Pattern (Component Side) - PMT1D-402 | 5-25 |
| Fig. 5-25: | Repeater Interface Board (A4) Circuit Pattern (Non-Component Side) - PMT1D-402 | 5-26 |
| Fig. 5-26: | Fault Locating Receiver Board (A5) Circuit Pattern (Component Side) - PMT1D-401 | 5-27 |
| Fig. 5-27: | Fault Locating Receiver Board (A5) Circuit Pattern (Non-Component Side) - PMT1D-401 | 5-28 |
| Fig. 5-28: | DET IN Receiver Board (A6) Circuit Pattern (Component Side) - PMT1D-404 | 5-29 |
| Fig. 5-29: | DET IN Receiver Board (A6) Circuit Pattern (Non-Component Side) - PMT1D-404 | 5-30 |
| Fig. 5-30: | Meter Interface Board (A7) Circuit Pattern (Non-Component Side) - PMT1D-407 | 5-31 |
| Fig. 5-31: | Power Supply Board (A8) Circuit Pattern (Component Side) - PMT1D-409 | 5-32 |
| Fig. 5-32: | Power Supply Board (A8) Circuit Pattern (Non-Component Side) - PMT1D-409 | 5-33 |

## LIST OF TABLES


| | | Page |
|---|---|---|
| Table 2-1: | Audio Freq. Vs. Filter Switch Setting | 2-5 |
| Table 2-2: | Signal Increase vs. Stress Level | 2-5 |
| Table 3-1: | Approximation Error | 3-14 |

# 1.0 INTRODUCTION

## 1.1 Description

The KS-22424 L1 Test Set is a portable, AC powered instrument intended for the testing and maintenance of T1D (3.152Mb/s, duobinary coded) digital carrier systems. The set contains a transmitter and receiver in one unit. The design includes three modes of operation. (Refer to Figure 1-1).

### 1.1.1 Fault Locating

The set isolates line troubles to a specific repeater section (maximum twelve repeaters from originating office). A DS1C signal and +5 Vdc are applied to the T1D digital line under test. The signal consists of a repetitive 64 bit word with selectable word patterns to vary the stress density level. The signal is inverted at twelve selectable audio rates. After the office repeater converts the DS1C signal to duobinary, the signal contains an audio tone (+5 Vdc disables the office repeater scrambler circuitry). The dB level of the audio tone is controlled by the stress density. This audio tone (unique to each apparatus case) is returned to the office from the apparatus case via a fault filter and loaded line. From the level of the returned tone, the condition of the repeater section can be determined. A synchronous detector is used in the test set receiver which allows for very narrow post detection bandwidths. A large receiver dynamic range and a receiver vernier make operation easy for the craftperson. Means are provided to measure the noise (300 Hz to 3 KHz Bandwidth) and resistance (TIP-GND, RING-GND and TIP-RING) on the fault locating line.

### 1.1.2 End-to-End Monitoring

A modified fault locating signal (scrambler not disabled) or an all ones DS1C signal is transmitted to another office. Another set at the receiving office can monitor the presence of pulses, bipolar violations and/or the all ones condition (DS1C DET IN jack).

### 1.1.3 Repeater Testing

The performance of office and line repeaters is verified prior to installation. When testing office repeaters, an all ones DS1C signal is applied to the repeater input, scrambled, and converted to duobinary at the repeater transmitting side output. This output signal is fed through one of three selectable artificial lines and looped back to the receiving side of the office repeater. The repeater restores the signal to the DS1C which is applied to the test set. When testing line repeaters, the test set scrambles and converts the DS1C signal to duobinary. This signal (with or without a 788 KHz square wave energizing the repeater side not under test) is fed through one of three selectable artificial lines and applied to the repeater input. The repeater output is applied to the test set which restores the signal to DS1C. Indicators are provided to monitor:

(a) The presence of pulses;
(b) bipolar violations;
(c) the all ones condition;
(d) repeater currents and voltages;
(e) Resistance between repeater circuitry and earth ground;
(f) the repeater fault locate circuitry.

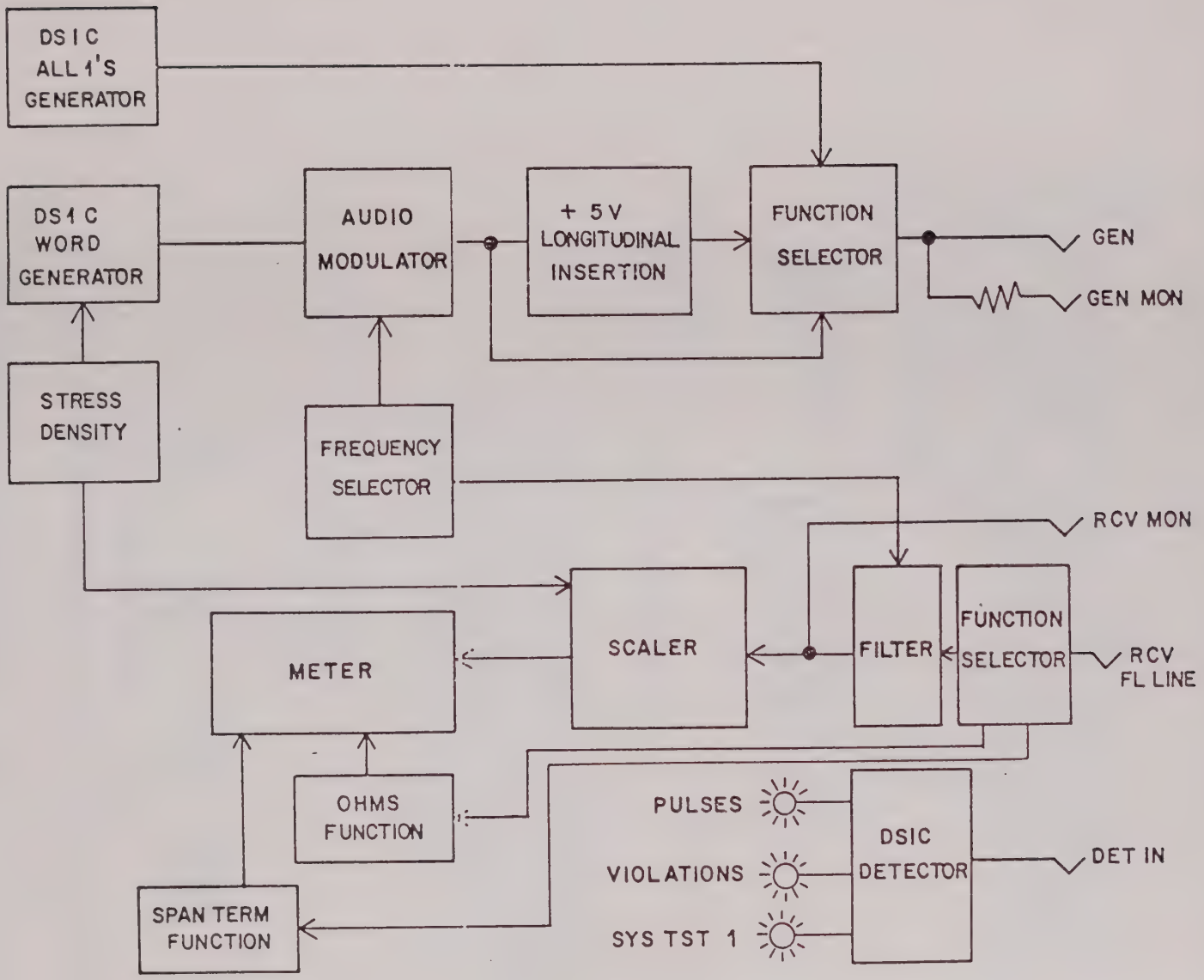



Fig. 1-1: Basic Fault Location Set Functional Block Diagram

1.1.4 The KS-22424 L5 and L6 are interchangeable adapters for testing 258 and 259 line repeaters, and the 260 office repeater, respectively. These adapters are furnished with the L1 test set.

1.2 Scope

This manual contains descriptive details of the KS-22424 Test Set plus related applications notes, maintenance information, diagrams, and parts information. The descriptive details are reduced to categories of physical and functional specifications, operating procedures, and operating principles. The manual's purpose is to provide sufficient familiarization to enable effective use and proper maintenance of the Test Set.

1.3 Summary Of Specifications

Transmitter

| | |
|---|---|
| Output Impedance | 100 ohm ± 10% |
| Output Level | 3 ± 0.3V p-p into 100 ohms |
| Frequency | 3.152 mHz ± 50 Hz |
| Pulse Width | 159 nsec ± 20 nsec |

Pulse Patterns

SYS TST 1
RPTR TST 1 } All Ones DS1C Pattern
RPTR TST 2

SYS TST 2 - repetitive DS1C sequence of eight 8 bit words. The words are either A words or B words depending on the stress density setting. Stress level one consists of 3 B words and 5 A words, and level six consists of 8 B words. One-zero invertions are inserted at twice the audio frequency. Simultaneously, 5V ± 5% is applied longitudinally on TIP and RING relative to the sleeve.

NOTE: A word = (11011000)
B word = (11010100)

Audio Frequency (Hz)

| | | | |
|---|---|---|---|
| A 832 | D 1206 | G 1722 | K 2413 |
| B 928 | E 1340 | H 2008 | L 2680 |
| C 1048 | F 1508 | J 2193 | M 3017 |

Audio Frequency Accuracy - ± 0.2%

FL - Same as SYS TST 2 except the 5 volt signal is removed.

DS1C Receiver

Input Impedance - 100 ohm ± 10%
Receiver Sensitivity - .6V to 12V p-p (up to 750 ft of office cable)

Receiver Outputs

PULSES LED
VIOLATIONS LED
SYS TST 1 LED (0 in all ones pattern will extinguish LED).

Fault Locating Receiver

| | |
|---|---|
| Input Impedance | 900 ohm ± 10% |
| Filter Frequency | Same as Audio Frequency Transmitted |
| Receiver Type | Synchronous |
| Detector Bandwidth | < 4 Hz |

Receiver Sensitivity 0 to -100 dBm (Into 900 ohms) in 10 dB steps

Receiver Accuracy ± 1 dB @ -40 to -80 dBm level
± 2 dB @ 0 to -40 dBm level
± 3 dB @ -80 to -100 dBm level

With S/N ratio in 4 Hz band around selected frequency of 15 dB minimum and in the 3 kHz band of -10 dB minimum.

Vernier Range 12 dB Min.

Meter Scale -20 to +1 dB

Span Term Noise Measurement

Bandwidth - 300 Hz - 3 kHz
Noise Measurement Range - 0 to - 100 dBm
Accuracy - See Fault Locating Receiver

FL Line Resistance Measurement

Zero is adjustable with front panel knob.
100 ohms to 20K ohms - Accuracy ± 5%.
Open circuit reads infinity on meter.

Repeater Tests

Artificial Lines
Short (-12 dB)
Med (-24 dB)
Long (-48 dB)
} loss at 1.576 MHz

Repeater Power
Simplex current source (20 - 150 ma at up to 24 volts), applied in either the A or B simplex path. (See Fig. 2-3).

Interference Signal
788 kHz (synchronous to signal) square wave ± 100 mV (200 mV p-p).

D.C. Voltmeter - 0 - 30V
Accuracy - ± 3%

D.C. Ammeter - 0 to 150 ma
Accuracy - ± 3%

Leakage Test - +130V DC current limited; 10 Megohm Decision Threshold.

Outputs - FL ABSENCE LED
LEAKAGE LED
SYS TST 1 LED
PULSE LED
VIOLATIONS LED

Operating Temperature - 0 to +50°C

Power Requirements - 115V AC ± 10% 50/60 Hz

Size (Nominal)
Height - 12.5 inches
Width - 15 inches
Depth - 12 inches
Weight - 26 pounds

# 2.0 OPERATION

## 2.1 Controls, Indicators and Connectors

2.1.1 FUNCTION Switch
Eight position rotary switch, which controls internal circuitry to perform the 8 functions.

2.1.2 OHMMETER Switch
Three position slide switch which determines the type of measurement made in the OHMS position.

2.1.3 OHMS SHORT Switch
Pushbutton momentary switch used in calibrating the ohmmeter. When depressed applies a short to the test set ohmmeter, but not the input to the FL LINE jack.

2.1.4 OHMS ZERO Adjustment
A knob used in conjunction with OHMS SHORT switch to zero the ohmmeter.

2.1.5 STRESS DENSITY Switch
Six position rotary switch operative in the SYS TEST 2 and FL positions (Function Sw.) only. Determines the number of A and B words (See Section 2.2.6) present in the eight word repetitive pattern. There are three B words followed by five A words in position one progressing to eight B words in position six. Also provides an increasing level of the transmitted FL signal and an increasing attenuation in the FL receiver as the density increases.

2.1.6 FILTER Switch
Twelve position rotary switch functional in the FL position only. Determines which of the audio tones the Fault Locating transmitter will generate and the Fault Locating receiver will recognize.

2.1.7 RECEIVER SENSITIVITY Switch
Nine position rotary switch operative in the SPAN TERM and FL positions only. Determines the amount of signal strength present in 10 dB increments. The signal level is equal to the dial setting added to the meter reading, provided the STRESS DENSITY switch is in Position One. In Fault Locating, the vernier (Sec. 2.1.8) must be in the CAL position for the absolute reading to be valid.

2.1.8 RECEIVER VERNIER Adjustment
Concentric knob in the RECEIVER SENSITIVITY switch. Functional only in the FL position. Allows the craftperson to adjust the meter indication over a minimum of 12 dB. This knob must be in the cal position (full clockwise) for FL readings to be absolutely accurate.

2.1.9 MILLIAMPS/VOLTS Switch
Two position slide switch used only in RPTR TST 1 and RPTR TST 2 positions. Determines whether the meter is displaying repeater voltage or current.

2.1.10 CURRENT ADJUST Adjustment
Knob determines the amount of current the internal current source will supply to the repeater.

2.1.11 ART LINE Switch
Three position rotary switch used only in the RPTR TST 1 and RPTR TST 2 positions. Determines the amount of loss the repeater input signal will experience during testing.

2.1.12 REPEATER TEST Switch
Five position rotary switch operable in the RPTR TST 1 and RPTR TST 2 positions. Set to type of repeater under test, LINE (UNI-or BI directional signal path) or OFFICE. Also in the LINE positions it selects which side of the repeater will be tested.

2.1.13 REPEATER POWER Switch
Two position rotary switch functional only in RPTR TST 1, RPTR TST 2, and LEAKAGE positions. Applicable only to line repeater testing, determines which of the powering paths (See Section 2.2.7.2) will be used.

2.1.14 FL ABSENCE LED
LED indicates if the repeater's fault locating winding is active. LED is forced on in RPTR TST 1, and functional in RPTR TST 2.

2.1.15 LEAKAGE LED
LED lights if repeater to earth leakage is excessive in leakage test. (10 Megohm Decision Threshold).

2.1.16 PULSES LED
LED will light if pulses are present. Active in repeater testing or whenever an input is present in the DS1C DET IN jack.

2.1.17 VIOLATIONS LED
LED will light if T1D errors are present in repeater testing, or if Bipolar violations (B.P.V.) are present in DS1C testing.

2.1.18 SYS TST 1 LED
LED is on if the T1D signal in repeater or system testing is a legitimate all ones pattern. Not functional in SYS TST 2.

2.1.19 115 VAC 50 - 60 Hz
Plug to supply A.C. power. A.C. line cord is provided and is carried in cover.

2.1.20 GEN MON
WECO Type 310 jack which provides a sample of the transmitted signal. Monitor signal level is -20 dB from transmitted signal when terminated in 100 ohms.

2.1.21 GEN OUT
WECO 310 jack from which the transmitted signal is obtained. Output impedance 100 ohms.

2.1.22 RCV FL LINE
WECO 310 type jack into which the Fault Line would be connected. Input impedance 900 ohms.

2.1.23 RCV MON
WECO 310 type jack at which the fault signal can be monitored in a 3 kHz bandwidth. The input signal is smaller than the monitor signal by the setting on the RECEIVER SENSITIVITY Switch (when in Stress Density One). Maximum drive capability 1000 ohms.

2.1.24 DS1C - DET IN
WECO 310 jack input to DS1C Type signal. Input impedance 100 ohms.

2.1.25 3AG 1/2A
Fuse holder.

## 2.2 Operational Description

2.2.1 General
This section provides an overview of the Test Set operation. Every position of the function switch will be described; block diagrams and waveforms are provided where required. This section should be used as a guide for Operating Instructions (Section 2.3) or an overview for the Theory Of Operation (Section 3.0).

2.2.2 OHMS
In this position a resistive measurement of an inactive input to the FL LINE input can be obtained. The jack connections to the fault locating receiver are broken so no internal impedance affects the reading. The top meter scale is in K ohms and covers the range of values expected to be encountered.

The OHMMETER slide switch is used in this position to select which of the three available readings is desired. An OHMS SHORT and OHMS ADJUST, as well as a mechanical zero are provided to enable calibration of the meter. Specifications call for an accuracy of $\pm$ 5%. There is no signal present at the transmitter output in this position.

2.2.3 SPAN TERM
In this position a wideband (300 Hz - 3 kHz) noise measurement of the fault line can be made. The noise level is read off the meter dB scale which covers a range from +1 dB to -20 dB. The reading is equal to the meter reading in dB + the receiver sensitivity setting. Thus noise can be measured from +1 dB to -100 dBm. The receiver sensitivity vernier is not functional in this position.

The actual noise signal is present at the RCV MON jack. The noise signal will be smaller than the signal at the monitor by the receiver sensitivity setting. For instance, if the meter reads 0 dB and the receiver sensitivity is set at -40, the noise level is -40 dBm (900 ohms) and the level at the RCV MON jack would be 0 dBm. The input impedance of the FL Line is 900 ohms, and the smallest resistive load which can be connected to the MON jack is 1000 ohms. No signal is transmitted in this position.

2.2.4 SYS TST 1

In this position a DS1C all ones pattern is available at the transmitter output. This signal can be monitored at the GEN MON jack. The signal at this jack will be 20 dB down from the transmitted signal if the load is 100 ohms.

2.2.5 SYS TST 2

The same pattern is transmitted as in the FL position except there is no 5V offset. No meter readings are possible in this position. All transmitted signal characteristics as described in Sec. 2.2.6 are valid. SYS TST 1 LED is inactive in this position.

2.2.6 FL

This is the fault locating position. The transmitted signal consists of a 64 bit DS1C repetitive pattern. The signal is riding on 5 VDC; this voltage disables the scrambler in the office repeater. Eight words, 8 bits in length comprise this pattern; the words are either A words or B words (See Fig. 2-1) and the ratio of B words to A words varies as a function of the STRESS DENSITY setting (See Figure 2-2). Increasing the stress level increases the level of the audio tone on the fault line (See Table 2-2).

Modulating this signal is an audio tone selected by the FILTER Switch (See Table 2-1). This tone causes a one-zero inversion at every transition of the audio frequency (2 X Freq. Audio). Thus when an audio transition occurs, if the next bit was supposed to be a one, it would be a zero and visa versa. These frequencies correspond to the fault locating filter frequencies on the line repeaters.

The fault locating receiver (FL LINE jack) is operative at this time. The fault signal level is read off the meter; the signal level in dBm (900 ohms) is equal to the meter reading + the RECEIVER SENSITIVITY switch position (Provided the vernier is in the cal position). The vernier is an attenuator which will vary the meter reading by a minimum of 12 dB. The vernier should only be used to attenuate signals which are on scale.

Varying the Stress Density increases the fault signal (See Table 2-2). The meter reading however will not change from one level to the next. This is because an attenuator pad at the receiver input is varied with stress level. The additional attenuation exactly ($\pm$ 0.2 dB) cancels out the expected signal gain. Therefore, to have an absolute reading of the fault signal, the vernier must be in the cal position and the STRESS DENSITY Switch must be in position one (REF).

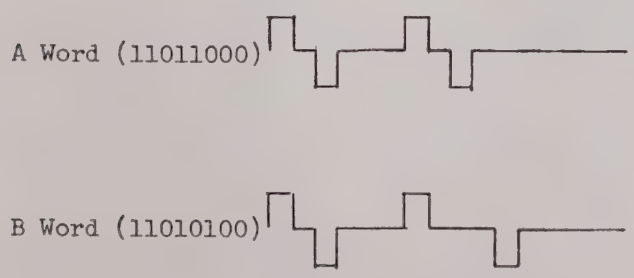



Fig. 2-1: Fault Locating Word Definition

| Stress Density Setting | 8 Word Pattern |
|---|---|
| 1 (REF) | B B B A A A A A |
| 2 | B B B B A A A A |
| 3 | B B B B B A A A |
| 4 | B B B B B B A A |
| 5 | B B B B B B B A |
| 6 | B B B B B B B B |

Fig 2-2: Word Organization vs. Stress Level

| Filter Switch Position | Freq. (Hz) | Filter Switch Position | Freq. (Hz) |
|---|---|---|---|
| A | 832 | G | 1722 |
| B | 928 | H | 2008 |
| C | 1048 | J | 2193 |
| D | 1206 | K | 2413 |
| E | 1340 | L | 2680 |
| F | 1508 | M | 3017 |

Table 2-1: Audio Freq. vs. Filter Switch Setting

| Stress Level | Signal Increase (dB) |
|---|---|
| 1 | 0 |
| 2 | 2.3 |
| 3 | 4.2 |
| 4 | 5.8 |
| 5 | 7.1 |
| 6 | 8.1 |

Table 2-2: Signal Increase vs. Stress Level

2.2.7 RPTR TST 1

2.2.7.1 General

Both Line and Office Repeaters are tested in this position. Power is applied to the repeater with a current source (20 - 150 ma) and the amount of current can be adjusted using the CURRENT ADJUST knob. Both repeater current and voltage can be read on the meter in this position. Whether the meter is displaying current or voltage depends upon the position of the MILLIAMPS/VOLTS Switch. The transmitter generates a DS1C all ones pattern. Exactly how this signal is used depends on the REPEATER TEST Switch.

2.2.7.2 Repeater Power

When the REPEATER TEST Switch is in the OFFICE position the current source is applied directly to the repeater power pins. Line repeater powering, however, depends on the position of the REPEATER POWER Switch (See Fig. 2-4).

Care must be taken in powering line repeaters since any line repeater will operate properly in either of the two positions. The full simplex path, however, will only be checked in the proper position. A faulty repeater could pass if tested in the wrong power position.

2.2.7.3 Line Repeater Testing

The first four positions of the REPEATER TEST Switch apply to line testing. Major headings UNI-DIR and BI-DIR are set depending on the type of line repeater under test (Fig. 2-3). The other heading SIDE 1, SIDE 2 determines where the T1D signal is applied. An interference signal is fed to the side not being tested.

The amount of attenuation between the T1D source and the repeater input is a function of the ART LINE Switch. The repeater output is monitored for PULSES, VIOLATIONS, and SYS TST 1 (all ones signal). The side not under test is terminated in a one hundred ohm load. The FL ABSENCE light is held on in this position. A block diagram of the line repeater test is shown in Fig. 2-5.

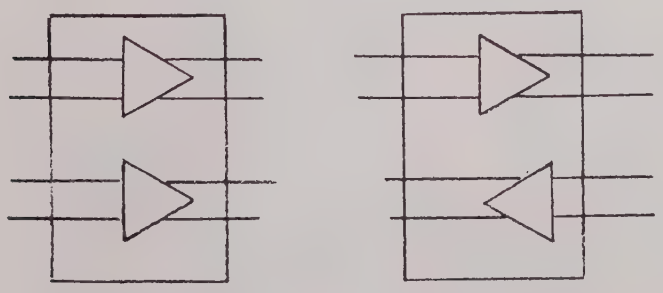



Fig. 2-3: Line Repeater Configurations

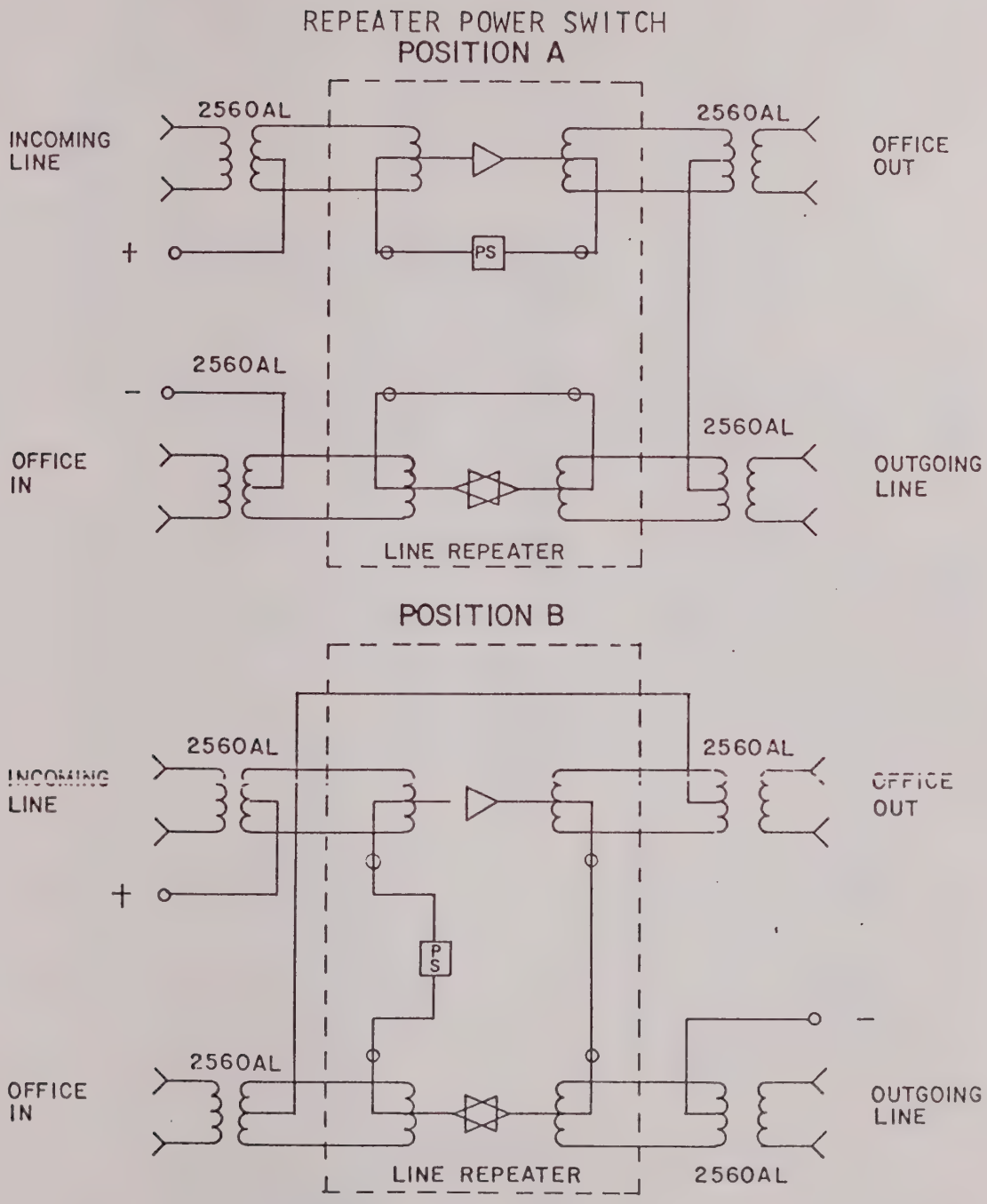



Fig. 2-4: T1D Line Repeater Power Circuit

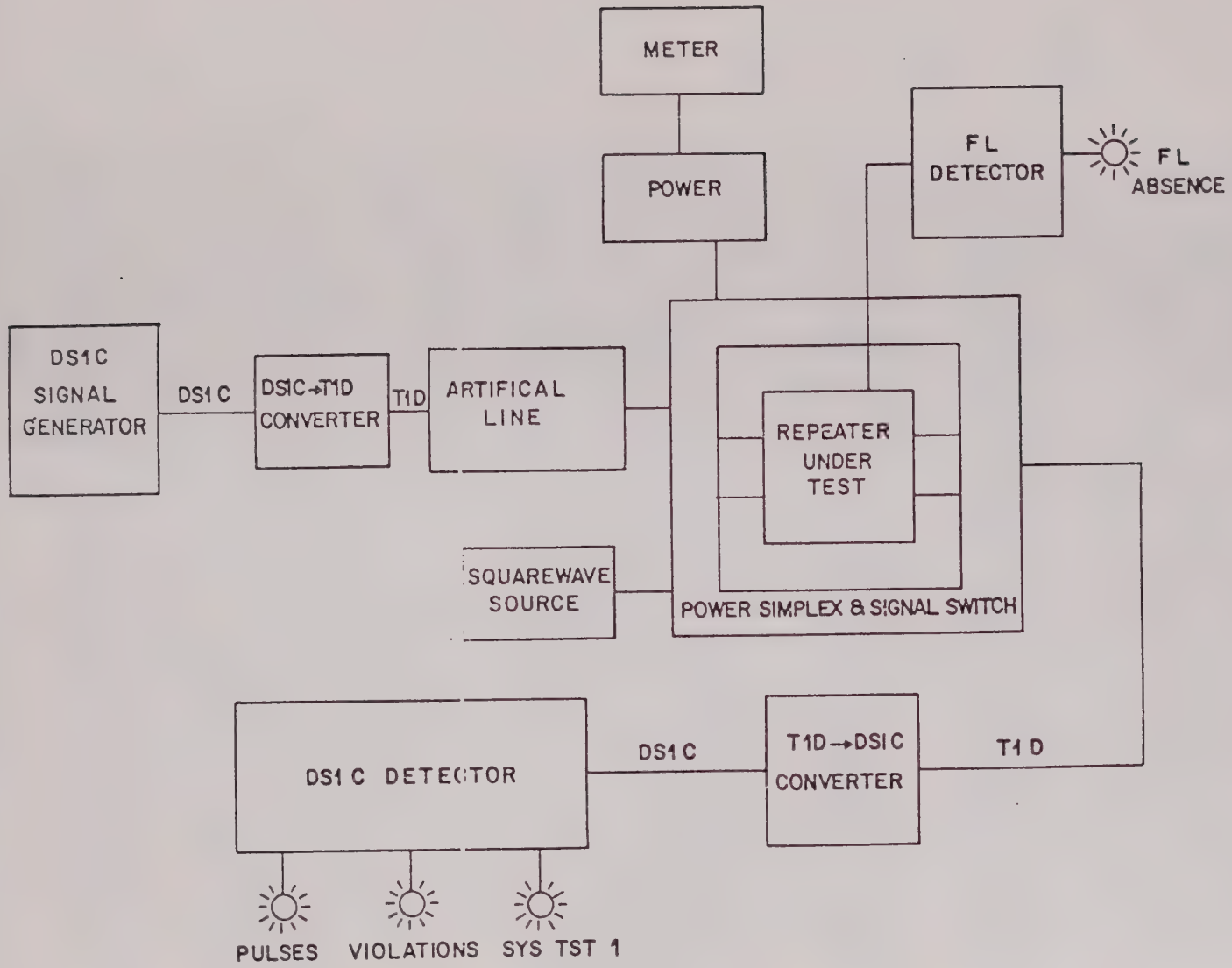



Fig. 2-5: Typical Line Repeater Test Arrangement

2.2.7.4 Office Repeater Testing (See Fig. 2-6)
In office repeater testing the signal path is different than in line repeater testing. An office repeater has both a DS1C side and a T1D side, the DS1C signal generated by the test set is converted to T1D in the office repeater. The signal is then attenuated as a function of the ART LINE Switch and fed back to the office repeater T1D input. The office repeater DS1C output is monitored for errors as in the line repeater position. No interference signal is present in office testing.

2.2.8 RPTR TST 2
The only difference between RPTR TST 2 and RPTR TST 1 is that the former has no interference signal in line repeater testing and the FL ABSENCE Indicator is active. This Indicator LED lights if the line repeater's fault locating circuitry is not operating properly.

2.2.9 LEAKAGE
In this position a 130V DC is applied to all of the line repeater's input and output pins. The amount of leakage to ground is measured. If the impedance to ground is less than 10 megohms, the LEAKAGE LED will light. There is no leakage test in the office position.

2.2.10 DS1C DET IN
This jack is a DS1C receiver capable of testing a signal down 20 dB from the DS1C level. Three indications are available, Active Line (PULSES), Bipolar Violations (VIOLATIONS) and All Ones Signal (SYS TST 1). This jack is operative in all positions of the FUNCTION Switch. Since the indicators used for DS1C Type signal testing are also used for T1D repeater testing it is important that no input to the DS1C jack be present during repeater testing. If a plug is in the DS1C jack when a repeater is also in the repeater slot, the indications apply to the plug and not the repeater. SYS TST 1 LED is not operative when the FUNCTION Switch is in the SYS TST 2 position.

2.3 Operating Instructions

2.3.1 General
Plug in test set, turn power on. POWER Switch should light.

2.3.2 Line Resistance Measurement

2.3.2.1 Put FUNCTION Switch in OHMS position. OHMMETER Switch in TIP-GND position.

2.3.2.2 Check meter reading on K ohm scale. If not on $\infty$ adjust mechanical zero.

2.3.2.3 Press in OHMS SHORT Switch. Meter should read zero.

2.3.2.4 If meter doesn't read zero, adjust with OHMS ZERO knob with OHMS SHORT still depressed. (Note: The Ohmmeter is shorted. The FL line is not shorted.).

2.3.2.5 Plug in FL LINE.

2.3.2.6 Set OHMMETER Switch to desired reading (TIP-GND, RING-GND, TIP-RING).

2.3.2.7 Read resistance on meter.

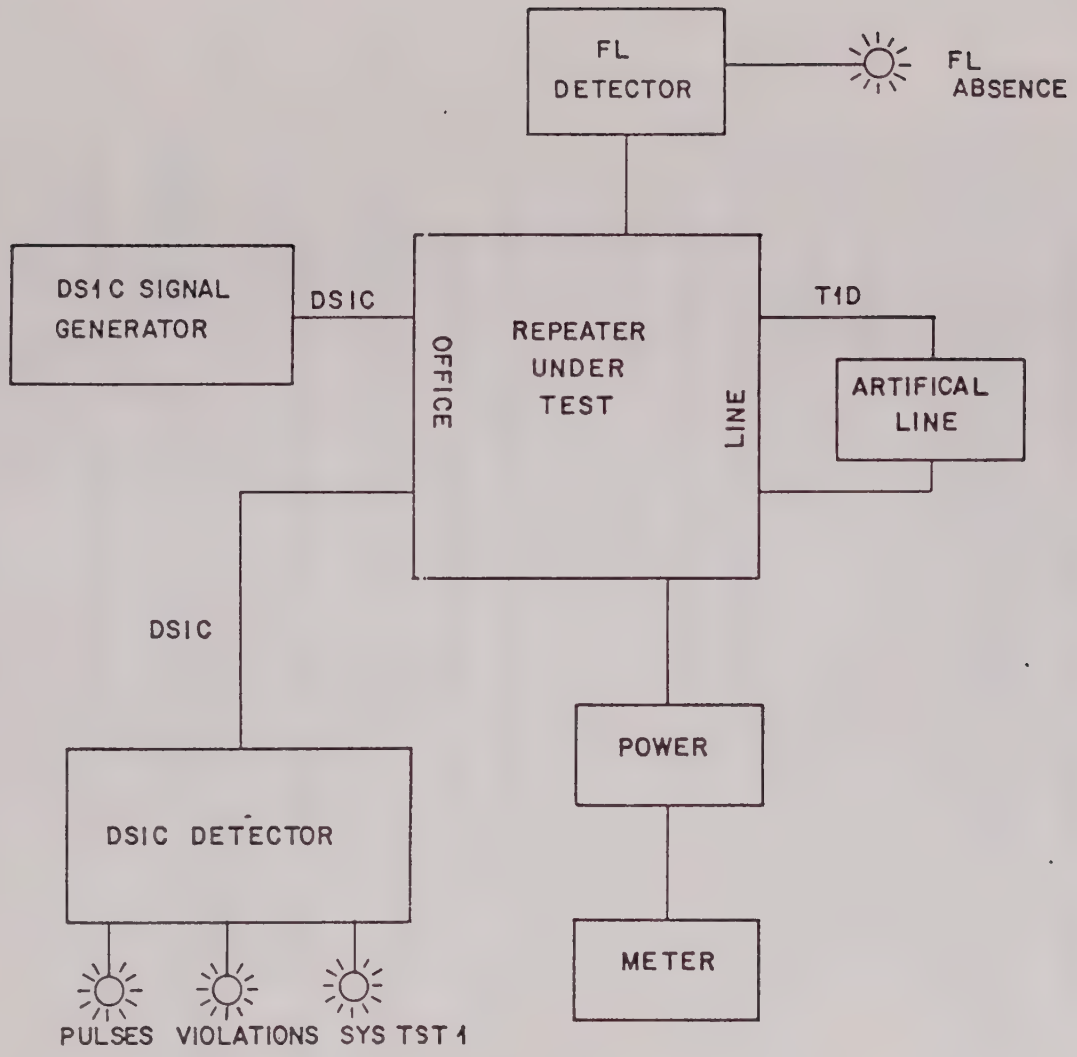



Fig. 2-6: Typical Office Repeater Test Arrangement

2.3.3 Line Noise Measurement

2.3.3.1 Set FUNCTION Switch to SPAN TERM.

2.3.3.2 Set RECEIVER SENSITIVITY Switch to 0 CAL.

2.3.3.3 Plug line into FL LINE Jack.

2.3.3.4 Turn RECEIVER SENSITIVITY Switch until reading is between +1 dB and -10 dB.

2.3.3.5 Noise level is meter reading + receiver sensitivity setting. (e.g. meter = -7, RECEIVER SENSITIVITY Switch = -40, Noise is -47 dBm (900 ohms).

2.3.4 Fault Locating Tests

2.3.4.1 Set FUNCTION Switch to FL.

2.3.4.2 Plug in line under test to GEN OUT Jack.

2.3.4.3 Plug in FAULT Line to RCV FL LINE Jack.

2.3.4.4 Set STRESS Switch to 1 (REF).

2.3.4.5 Set RECEIVER SENSITIVITY Switch to 0 CAL.

2.3.4.6 Set RECEIVER VERNIER Pot full clockwise (CAL).

2.3.4.7 Set FILTER Switch to desired setting (A - M).

2.3.4.8 Check that RECEIVER SENSITIVITY vernier is Full clockwise (CAL position).

2.3.4.9 Turn RECEIVER SENSITIVITY switch until reading is between +1 dB and -10 dB.

2.3.4.10 Signal level is meter reading plus RECEIVER SENSITIVITY setting (e.g. Meter = -7, RECEIVER SENSITIVITY Switch = -40, Signal = -47 dBm (900 ohms)).

2.3.4.11 Adjust vernier to convenient reading on meter.

2.3.4.12 Set STRESS DENSITY Switch to next highest level. Allow meter to settle.

2.3.4.13 Meter reading should not vary greater than $\pm$ 1 dB.

Repeat 2.3.4.12 - 2.3.4.13 for STRESS DENSITY Positions 3 through 6.

For additional filter settings, restart at 2.3.4.4.

2.3.5 Repeater Testing (RPTR TST 1)

2.3.5.1 Set FUNCTION Switch to RPTR TST 1.

2.3.5.2 Be sure there are no plugs in either GEN OUT or DS1C DET IN Jacks.

2.3.5.3 Use correct adapter in repeater housing for repeater type under test.

2.3.5.4 Select proper powering using REPEATER POWER Switch.

2.3.5.5 Select proper type of testing for repeater under test using REPEATER TEST Switch (i.e. UNI-DIR for Uni-direction, BI-DIR for Bi-directional or OFFICE for office repeater).

2.3.5.6 If line repeater, start with SIDE 2.

2.3.5.7 Set ART LINE for SHORT.

2.3.5.8 Set MILLIAMPS/VOLTS TO MILLIAMPS.

2.3.5.9 Set CURRENT ADJUST fully counter-clockwise.

2.3.5.10 Plug in repeater.

2.3.5.11 Adjust CURRENT ADJUST until meter reads approximately 120 ma. (Red line on meter).

2.3.5.12 Place MILLIAMPS/VOLTS in the VOLTS Position.

2.3.5.13 The reading should be approximately 11 volts for line repeaters and approximately 22 volts for office repeaters.

2.3.5.14 A good repeater will have only the following LEDs on - PULSES, FL ABSENCE, SYS TST 1.

2.3.5.15 Set ART LINE for LONG, if line repeater. Set ART LINE for MEDIUM if office repeater.

2.3.5.16 A good repeater will have the following LEDs on - PULSES, FL ABSENCE, SYS TST 1. (Note: Other LEDs might flash momentarily when ART LINE Switch is changed). This completes the test for an office repeater. Continue to the next step to complete the line repeater test.

2.3.5.17 Set REPEATER TEST Switch to SIDE 1 and ART LINE to SHORT. Repeat Steps 2.3.5.14 - 2.3.5.16.

2.3.5.18 For testing additional repeaters, start at 2.3.5.3.

2.3.6 Repeater Testing (RPTR TST 2)

Same as RPTR TST 1 except a good repeater will have only the following LEDs on - PULSES, SYS TST 1. (Replaces 2.3.5.14 and 2.3.5.16).

2.3.7 Line Repeater Leakage Testing

2.3.7.1 Set FUNCTION Switch to LEAKAGE.

2.3.7.2 Insert repeater. For a good repeater the LEAKAGE LED will be off.

2.3.7.3 Remove repeater. LEAKAGE LED should light.

2.3.8 Other FUNCTION Switch Positions

2.3.8.1 SYS TST 1 - DS1C ALL ONES Signal is available at GEN OUT output.

2.3.8.2 SYS TST 2 - Fault Locating signal without 5 VDC at GEN OUT. STRESS DENSITY and FILTER Switches will affect signal just as in FL Position.

2.3.9 Use of DS1C Receiver

2.3.9.1 Plug DS1C Type signal into DS1C DET IN Jack. The PULSES, SYS TST 1 (All Ones), and VIOLATIONS LEDs provide indication of the signal status.

2.3.9.2 SYS TST 1 LED will not function in SYS TST 2 position of the FUNCTION Switch.

2.3.9.3 Indicators

2.3.9.3.1 PULSES - indicates an active line

2.3.9.3.2 VIOLATIONS - on or blinking if Bipolar Violations occurring.

2.3.9.3.3 SYS TST 1 - on if signal is all ones (except if FUNCTION Switch in SYS TST 2).

2.3.10 Use of Monitor Jacks

2.3.10.1 GEN MON - allows monitoring of transmitted signal. Signal level will be 20 dB down from transmitted signal if monitoring impedance is 100 ohms.

2.3.10.2 RCV MON - allows monitoring of input to RCV FL LINE Jack (Refer to Sections 2.1.23 and 2.2.3).

# 3.0 THEORY OF OPERATION

## 3.1 Overview

This section describes the circuitry on the eight Printed Circuit boards used in the KS-22424 L1 Test Set. Block diagrams are provided where applicable along with schematics and component designation. System block diagrams are given in Fig. 3-1 and Fig. 3-2.

## 3.2 A1 Transmitter Board (Schematic 5-3)

### 3.2.1 General

The transmitter card generates all signals used in repeater testing and fault locating. There are basically only three output signals; an all ones pattern, a fault locating signal, and 788 kHz interference signal. A block diagram of the transmitter is given in Fig. 3-3.

### 3.2.2 Timing

The basic timing for the KS-22424 L1 Test Set is derived from two crystal oscillators. The first consists of U7 and a crystal (X1) which form a 6.304 MHz oscillator providing the base for the system clock. It feeds U12 - a divide by two and divide by four circuit. Dividing by two produces a 50% duty cycle clock at 3.152 MHz, which is then divided by four to produce the required 788 KHz interference signal. This signal, derived as it is from the system clock, is synchronous with the transmitted signal.

### 3.2.3 Signal Generation

U23A is a D-flip-flop which determines whether the output signal will be all ones, all zeros, or the fault locating signal. When a ground is applied to the Span TERM input (C) this holds the FF in the clear position, and its output is a zero. If the Span Term is high and all ones input (Pin 3) is grounded, the FF is set and the output is held at a one. The output of U23 is one input to U22-A which with U17-A forms an AND gate. The other input to U23-A is the system clock. Thus when the clock goes high if the data is a one, the output of U17-A goes high. This in turn clocks U23-B which acts as a data latch whose state changes on each clock pulse. U24 is a driver for the output transformer (T1). It is basically two AND gates: the output of one tied to the transformer + input and the output of the other tied to the transformers - input. One input to one of these ANDs is the Q output of U23-B and one input to the other AND is $\overline{Q}$ output of U23-B. Thus on every one clocked into U23-B one AND can be enabled and the other cannot. Since U23-B flips on every data one, the drivers in U24 alternate being enabled. This converts the $T^2L$ signal to bipolar since the transformer is driven first from one end and then the other.
The other input to the AND is common to both AND gates. U22-B and U18-A form another AND gate. This gate ANDs the clock and data. This input provides the Return to Zero (RZ) characteristic of T1C since the transformer is driven on only for a half cycle.

The center tap of the T1 input side is connected to 5V adj. input (4) which is adjusted to give the proper output level. The center tap of the output side is usually open circuited, but in the FL position

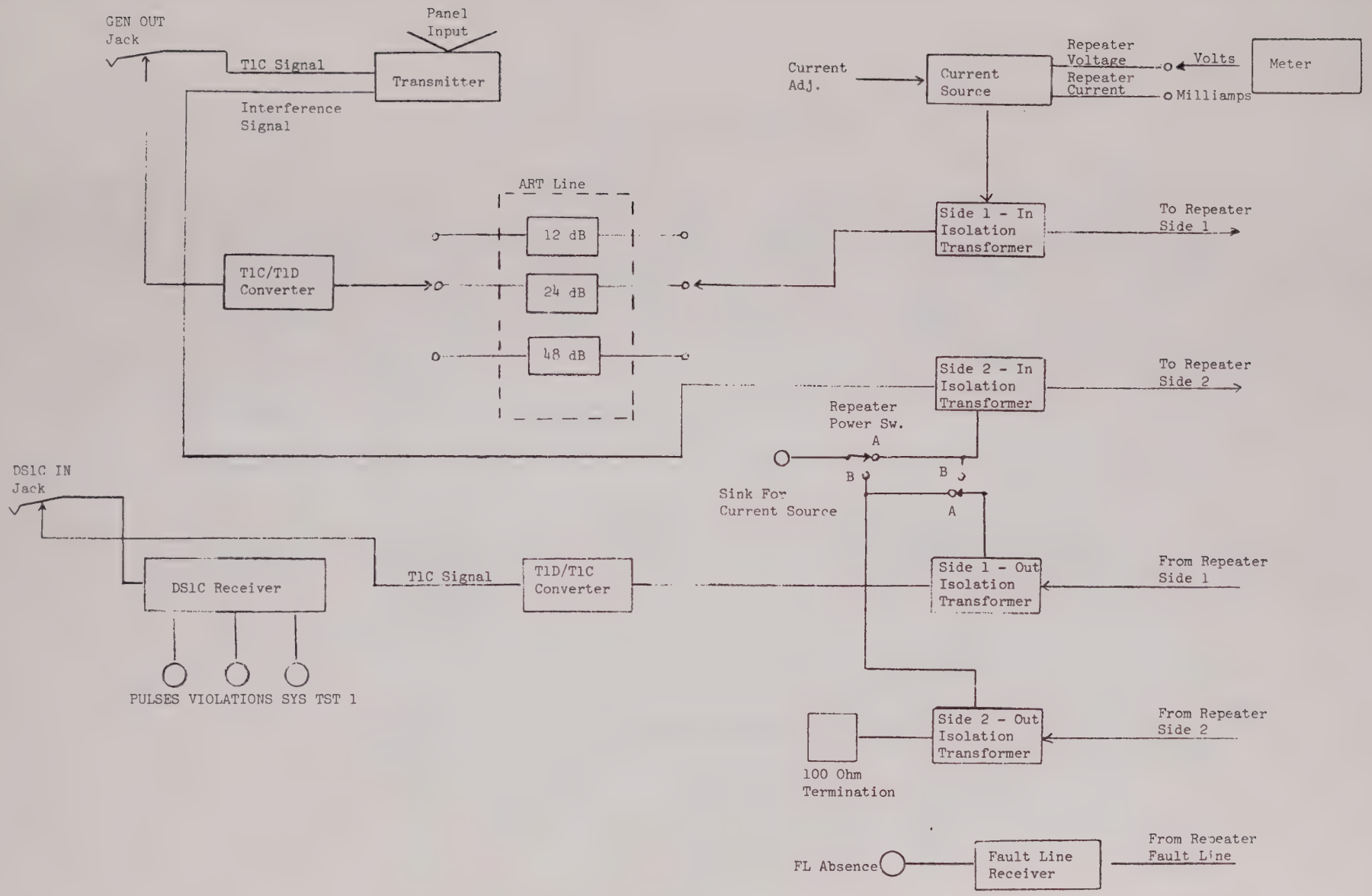



Fig. 3-1 Line Repeater Testing
Side One Selected RTPR TST 1

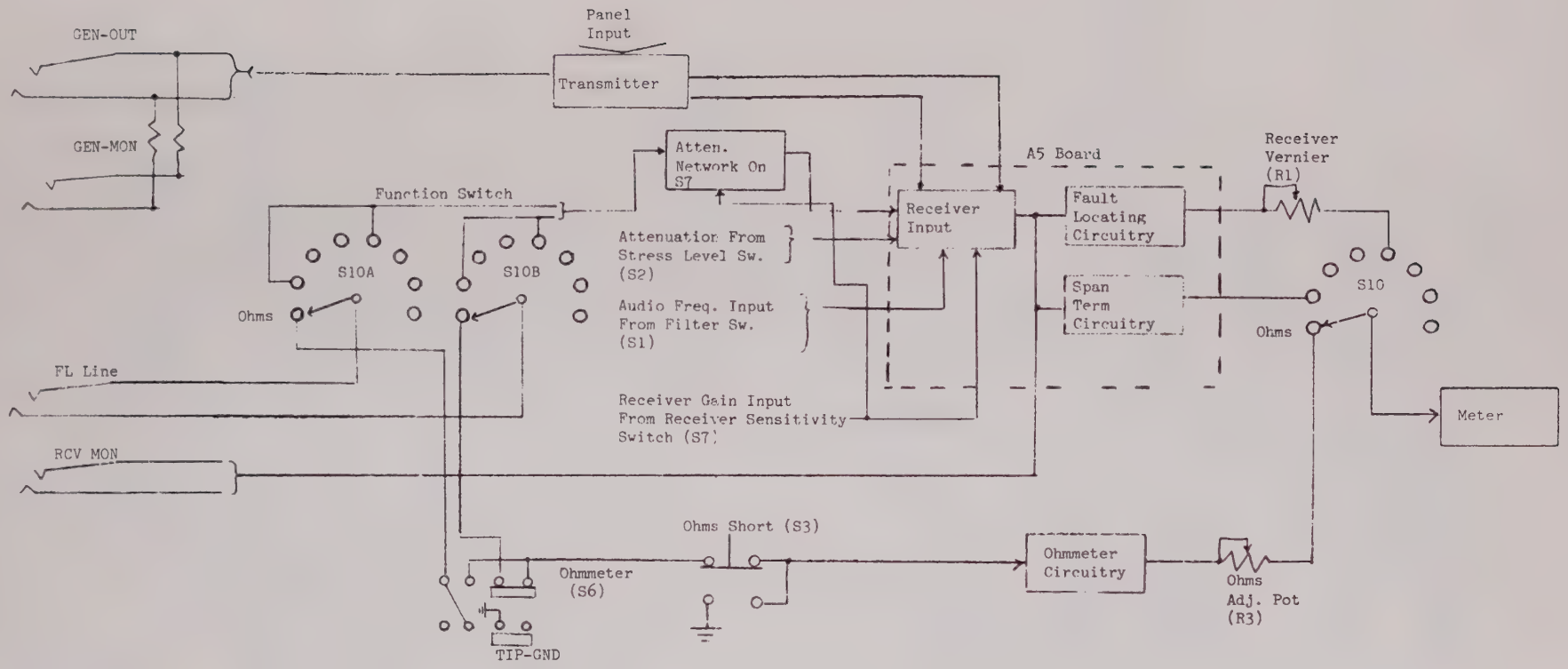
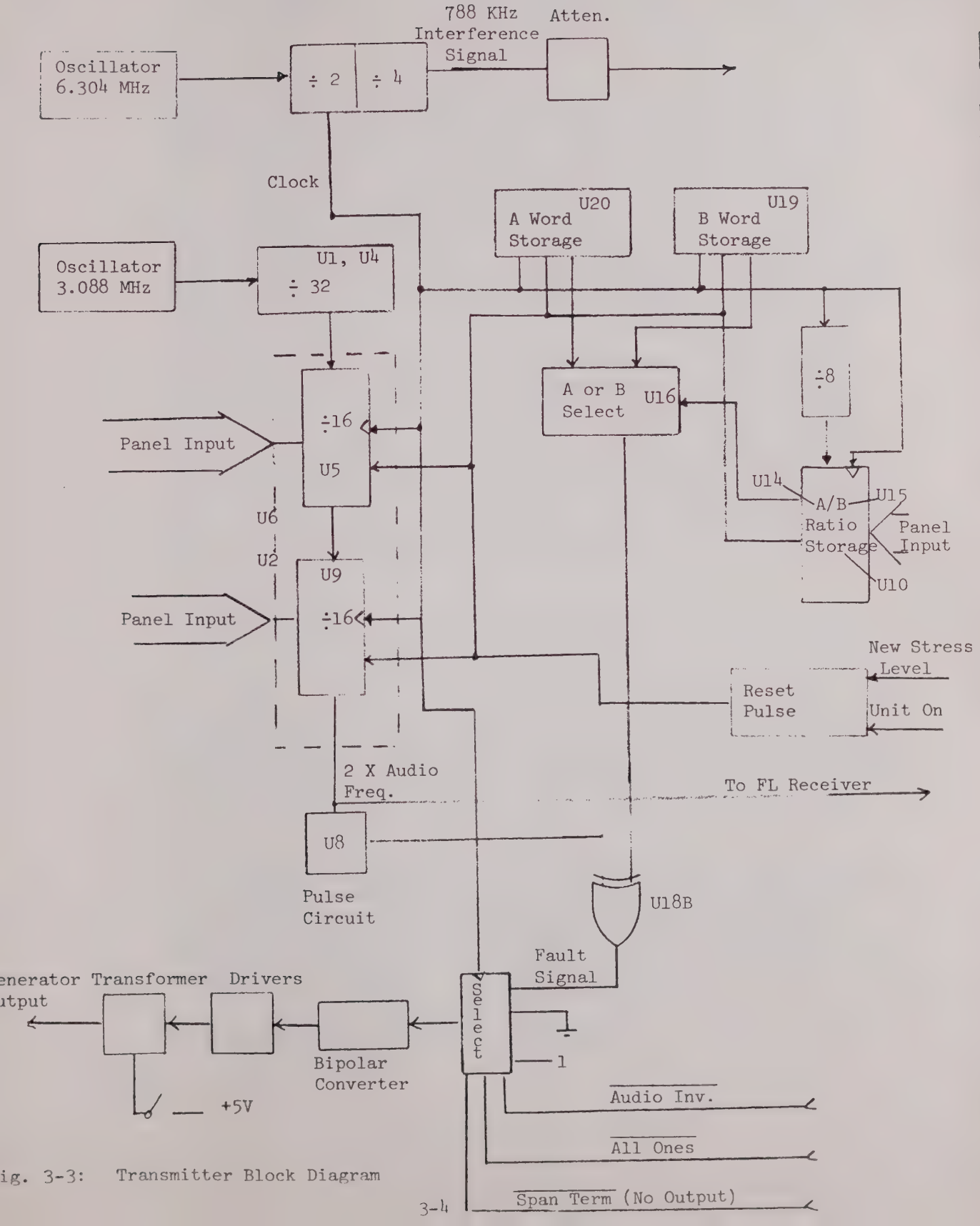



Fig. 3-2 Fault Locating Circuitry, Ohmmeter and Wideband Noise Circuitry




ig. 3-3: Transmitter Block Diagram

5 VDC is applied. This voltage is used to disable the office repeater scrambler without affecting the transmitted signal's A.C. characteristics. Resistors R9 and R10 are present to provide the proper output impedance (100 ohm).

3.2.4 Fault Locating Signal Word Structure

The majority of the remaining circuitry is used in generating the fault locating signal. The fault locating signal consists of a sixty-four bit repetitive sequence. This pattern can be interpreted as consisting of 8 eight-bit words which are either A or B words (See. 2.2.6); the ratio of which depends on the stress level (Fig. 2-2). U20 and U19 are parallel loaded serial shift registers, whose output is fed back to the input. This configuration acts as storage for the A and B words since the words keep shifting through repeatedly. The output of the two storage registers are fed to U16 which consists of four two line to one line data selectors. Depending on the sense of the select line either the A or B output appears at the U16 output.

The select line to U16 is another storage register which contains the A/B pattern*. This register is clocked by the system clock divided by eight or once per word. The pattern in this register is set by the outputs of U15 and U10. These chips are eight lines to three lines priority encoders which put out a different 3 bit binary word depending on which of its 8 input lines is grounded. The stress density switch grounds one input to each of the chips, thus setting up a six bit binary word at the output. A third input from the stress level switch gives a seventh bit, and since there is always at least one A word only seven bits are necessary.

3.2.5 One/Zero Inversions

In addition to the word structure there are one/zero inversions in the pattern spaced at one of 16 audio rates (Table 2-1). The generation selection and insertion of these rates will now be discussed.

U3, X2 and the associated circuitry form a 3.088 mHz oscillator which is the basis for the audio frequency. U1 and U4 provide a fixed divide by 32 circuit which gives a frequency of 96.5 kHz. U5 and U9 are presettable synchronous 4 bit binary counters. They are arranged to count down to zero; but will count down from 256 to the presettable binary input thus truncating its count. By setting the input, the counter will therefore divide by anywhere from 1 to 256.

The binary input is derived from U6 and U2, 8 line to 3 line decoders as discussed in setting up the A/B word ratio. These binary words are controlled by the FILTER Switch and change for each position. The binary words are selected to give frequencies as close as possible ($\pm$ 0.2%) to twice the audio frequencies. The output of the truncated count circuit is fed to U8, a dual D flop. The two flip-flops

*e.g. 11100000 for 3B and 5A, or 11110000 for 4 of each.

are set up to have an output which will go high for one full system cycle and then go low until the next positive edge of the audio frequency. This output is one input to an XOR (U18-B), while the other input is the fault locating signal. As long as the output of the flip-flops is zero the fault locating frequency passes through unchanged. When the flip-flop output goes high the sense of the fault signal is reversed (i.e. a one becomes a zero and vice versa). Since the input signal is twice the filter frequency and the flip-flop output lasts only 1 cycle there is one one-zero inversion each half cycle of the audio frequency.

3.2.6 Power Up and Reset

The other circuitry on the transmitter board consists of a power up or reset generator and a stress level reset signal. U21 is a comparator: one input of which is a resistor divider to +5V, and the other input is a resistor cap (R6, C17) to +5 volts. When the set is initially turned on the side with the R, C will be held low longer than the other side. Therefore the output will pulse high. This signal is used to set all registers on the transmitter board and some flip-flops on the fault line receiver board. In addition, all registers involved in generating the stress level word ratio must be reset with every new setting of the STRESS DENSITY Switch. This is accomplished by U11 which is a 556 dual timer set up as a monostable. When the STRESS DENSITY Switch is turned, the stress reset line (12) is momentarily open circuited. This is capacitively coupled to the input of the 556 which remains high. When the STRESS DENSITY Switch closes in the next setting it couples a low to the input to the monostable. This causes the output to go high long enough to reset the stress level registers.

## 3.3 A4 Repeater Interface Board (Schematic 5-6)

3.3.1 General

The repeater interface board (Fig. 3-4) provides several distinct functions relating to repeater testing. The current source used to power repeaters is housed on this board. All the buffer transformers used to drive and isolate repeater inputs and outputs are contained on the A4 board. The gain block for monitoring and displaying repeater current and voltage are on the A4 card. In addition, the receivers and detectors for FL absence and excess leakage are housed on the repeater interface board.

3.3.2 Constant Current Source

The simplex circuitry in the repeaters is powered via a constant current source. The constant current source is capable of delivering 20 - 150 ma at a maximum voltage of 24 volts. The open circuited voltage of the source never exceeds 30V. The source is built around VR1, a three terminal voltage regulator, which puts a constant voltage from its output pin to its reference pin. From its output to the reference pin is a potentiometer which is adjusted from the front panel. The reference point is used to drive the repeater thus, regardless of the repeater voltage, the voltage regulator's current output will be determined by the resistance of the potentiometer.

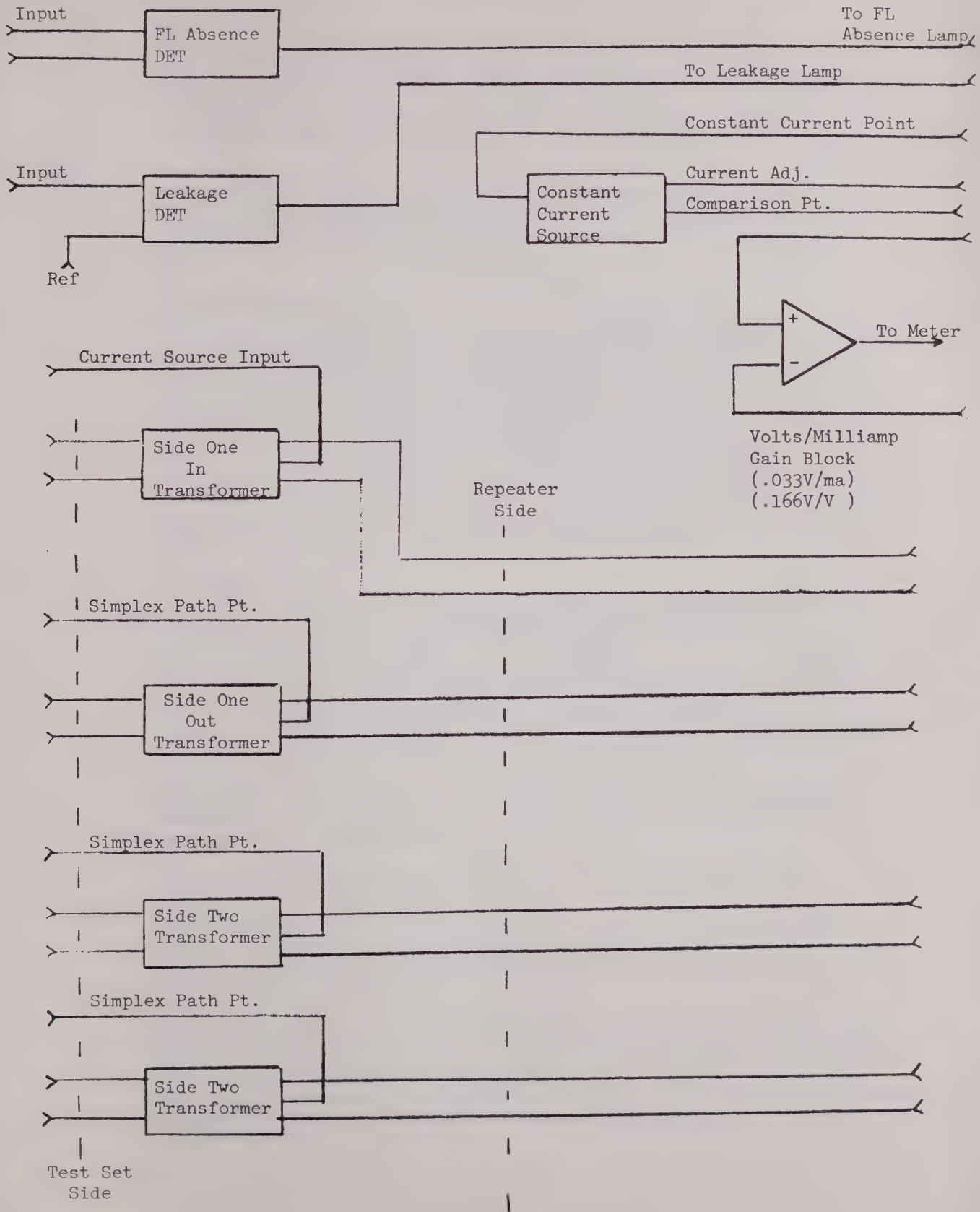



Fig. 3-4: Repeater Interface Block Diagram

3.3.3 Meter Interface

Monitoring of the repeaters is accomplished through U1-B. This amplifier monitors the voltage across the potentiometer in the current mode, and the voltage at the voltage regulator reference in the voltage mode. The input voltage is amplified and drives the meter. Whether current or voltage is displayed depends on the VOLTS/MILLIAMP Switch.

3.3.4 Repeater Interface

Transformers T1 - T4 are the input and output transformers which interface with the repeater under test. The center taps of these transformers on the repeater side are used in the simplex powering loop.

3.3.5 Leakage Measurement

U4 is a voltage comparator which is used in the leakage mode. In this position the simplex current is removed from the repeater and a 130 VDC signal applied. The amount of current flow to the case reference is then determined. The 130 VDC is applied to all input and output pins through a 1 meg resistor to limit the amount of current flow. The input points are then connected through the Function Switch to the input of U4. This input level is compared to a level equal to the level which would be present if the repeater were 10 megohm. If the voltage is less than this level, the repeater would be out of spec and the voltage comparator would be off, thus turning on the LEAKAGE LED. No leakage test is performed in the office position.

3.3.6 Active Fault Line

Detection of an active fault locating line is accomplished with the remaining circuitry on the board. Transformer T5 is the input to the repeater fault locating line. In conjunction with Q1 and associated circuitry it provides a high impedance (greater than 1K ohm impedance). U2-A and U2-B are high frequency op-amps providing 40 dB of gain. A tuned circuit, consisting of R27, L2, and C23, filters out signals outside the band of interest. U1a provides additional gain (20 dB) and isolates the tuned circuit from the peak detector (CR1, C26). The peak detector has a fairly fast discharge time constant (.1 sec) to allow for line spikes or noise. U3 is a comparator which, if the peak level is less than that corresponding to a 6 mVrms input signal, enables the FL ABSENCE LED.

3.4 A6 DET IN Receiver (Schematic 5-8)

3.4.1 Front End (Fig. 3-5)

The main purpose of the front end is to provide a 100 ohm (at T1C rates) input to the incoming signal and provide $T^2L$ compatable signals to the processing circuitry.

The input signal is transformer coupled (T2) to the gate of the input stage Q3. The transformer and FET combine to provide a high impedance. The output of the FET follower is capacitively coupled to the base of Q2, the gain of which is adjusted to 6 dB via select resistor R13 (nominally 2K ohm). The stage compensates for the loss through transformer T1.

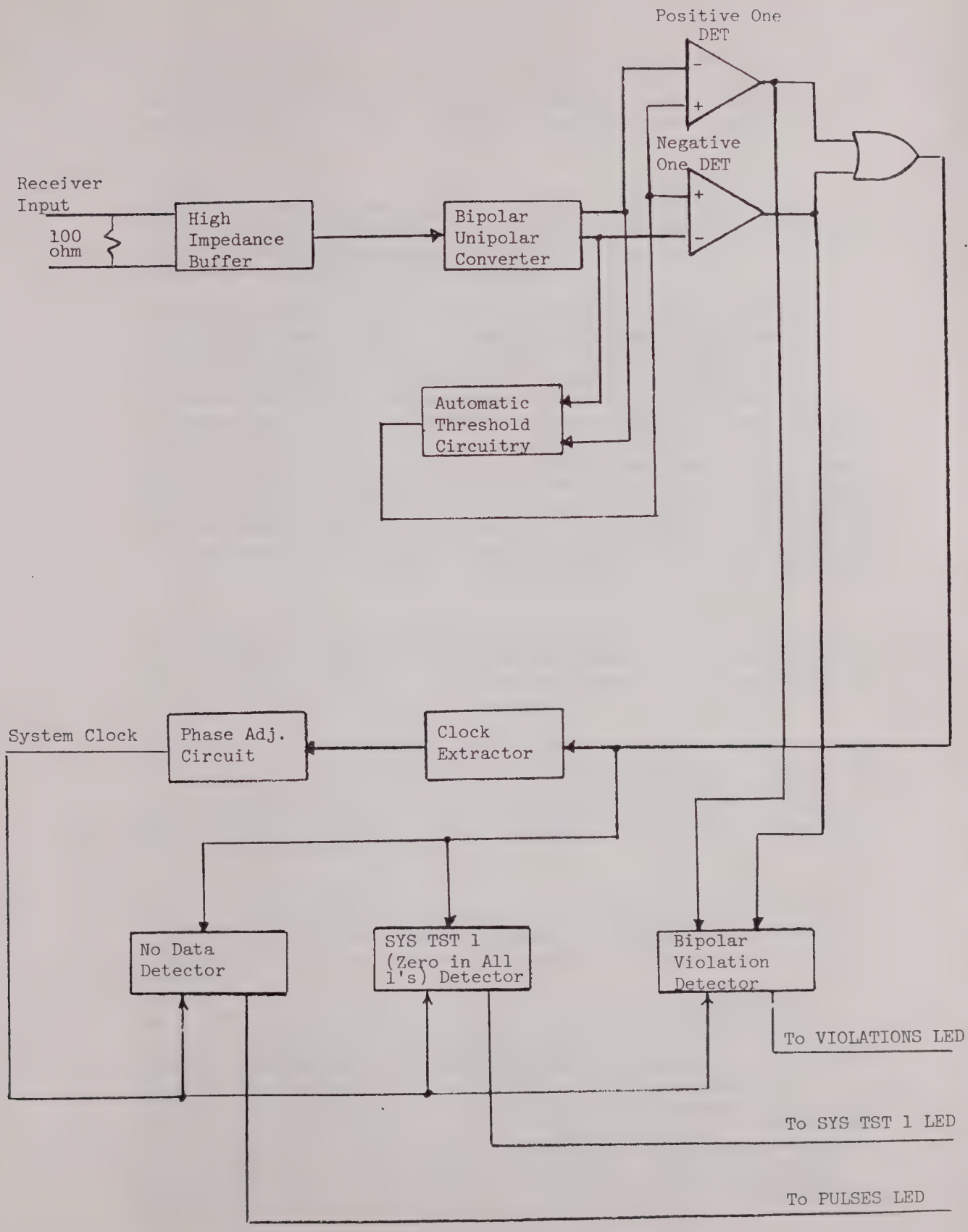



Fig. 3-5: DET IN Block Diagram

Emitter follower Q1 is used to drive transformer T1 which splits the incoming bipolar waveform into two waveforms 180° out of phase. One waveform consists of positive pulses for negative 1's and the other waveform is the inverse. These two signals are then fed to the slicer circuitry.

3.4.2 Slicer

The slicer combines two separate functions. First, it sets an amplitude threshold which recognizes a "1" or "0" logic data level. Second, it separates the positive and negative bipolar levles into two separate data signals which are $T^2L$ compatable.

Integrated circuit (U2) consists of five matched transistors, two of which (Q3, Q4 with C5 and R5) form a peak detector which is used as a reference for detection of a logic "1". Transistors Q1 and Q2 present high impedance loads to the transformer outputs and low impedance outputs to the comparator (U1). The fifth transistor Q5 is connected as a diode and is used to compensate for the Vbe loss across the other transistors. U1 consists of two comparator circuits. The negative inputs are tied together and to the peak detector's output. The positive inputs are fed from the two output pulse streams from U2 (Q1, Q2). The two outputs of this integrated circuit are now unipolar $T^2L$ compatable levels, one of which is from positive 1's and the other is from negative 1's. These lines (bipolar A and bipolar B) are used for clock extraction and all waveform analysis done on the T1C signal.

3.4.3 Clock Extraction

U3 consists of two monostables which are used to stretch the pulses which are approximately 50% duty cycle at the input. The outputs of U3 are OR'ed U7-A, U7-B and U8-A. This output feeds U12, another monostable, which is the input to the clock extractor.

The output of the monostable adds energy to the tank circuit driven by Q5. The tank circuit C26 and L2 is tuned to 3.152 mHz. Pulsing this high Q circuit causes it to ring at its characteristic frequency. The tank circuit drives a darlington pair (Q6, Q7) followed by a phase shift circuit and slicer (U4). The output of the slicer is the clock for all signal manipulation.

3.4.4 Bipolar Violation Detector

This circuit consists of two 2-stage binary counters (U5 and U9). A gate for each counter ANDs the receiver clock pulses with a slicer output to give Return to Zero (RZ) signals which toggle and reset the counters.

When a "1" of positive polarity is received, the first stage of one counter is set and the second counter is cleared. If the next "1" received is also of positive polarity, another count will be added to the first counter, indicating the occurrence of a violation. However, if the next "1" is of negative polarity, this counter will clear and a count of one will register in the first stage of the second counter. The output of the two counter chains are OR'ed and drive a monostable (U10-A). This circuit puts out a 100 msec pulse which turns the VIOLATIONS LED on when triggered. Thus if only one BPV occurs the LED on time is sufficient to be visible.

3.4.5 No Data Detector

The No Data Detector, consisting of U14, monitors the output of the slicers through U8-A. The dual retriggerable monostable multivibrator is connected in a tandem arrangement, where the second stage is triggered by an output of the first. The first stage is retriggered by data pulses from the output of the second stage. In the event that data is interrupted, retriggering is discontinued, permitting the circuit to time out. The time constant of the first stage (26.5 microseconds) is determined by circuit elements C31 and R43. This time constant corresponds to 82 $\pm$ 10 time slots. An output from this stage is applied to the input of the second stage which inhibits triggering of the first stage for a 100 ms period following detection of No Data. The 100 ms time constant is determined by components R44 and C32. CR1 is also required for proper circuit operation. The output of the No Data circuit is extracted from the first stage. This output is directed to both the PULSES indicator (Q4) and to U8-B. When No Data is detected, U8-B disables the clock extractor output until the data returns.

3.4.6 SYS TST 1

This circuit determines whether or not the data stream is an all ones pattern. U13 is a flip-flop, its input driven by U8-B. If the incoming data stream is all ones, U13's output will be a constant high. If a single zero exists in the stream it will be clocked into U13's output, thus triggering U10-B - a monostable. This circuit once triggered, will have a low output for a 100 msec duration independent of its input. This pulse turns the SYS TST 1 LED off (Q8).

## 3.5 A5 Fault Locating Receiver Board (Schematic 5-7)

3.5.1 General

The purpose of the Fault Locating Receiver (Fig. 3-6) board is to receive, amplify, and detect wide band noise in the Span Term position and fault locating signals in the FL position.

3.5.2 Input Stages

Transformer T1 on the A7 Meter Interface Board (Fig. 5-9) is the input to the fault locating receiver. It has a 1:1 turns ratio and provides a 1K ohm impedance to the fault line. U5 is a +20 dB buffer providing isolation between the input and the active filter (U4). The active filter is a double pole, low pass which has a loss of .1 dB at 3017 Hz, the highest fault locating frequency.

3.5.3 Programmable Gain

U10 is an operational amplifier and U11 is a quad analog switch. All four of the switches are connected in the feedback path of the amplifier, and depending on which switch is enabled, the closed loop gain varies. The maximum gain is 30 dB, the minimum is 0 dB (See Fig. 3-6). A similar circuit (U15 and U16) follows this initial programmable gain block. U20 is a unity gain amplifier. By selecting which line is grounded on each gain block, the gain can be varied from 0 dB to +60 dB. U19-B is a unity gain buffer which feeds the RCV MON jack. The buffer output is an amplified (Receiver Sensitivity), bandlimited (3 kHz) representation of the input line signal. At this point, the signal paths diverge dependent upon whether the set is in the Span Term or FL position.

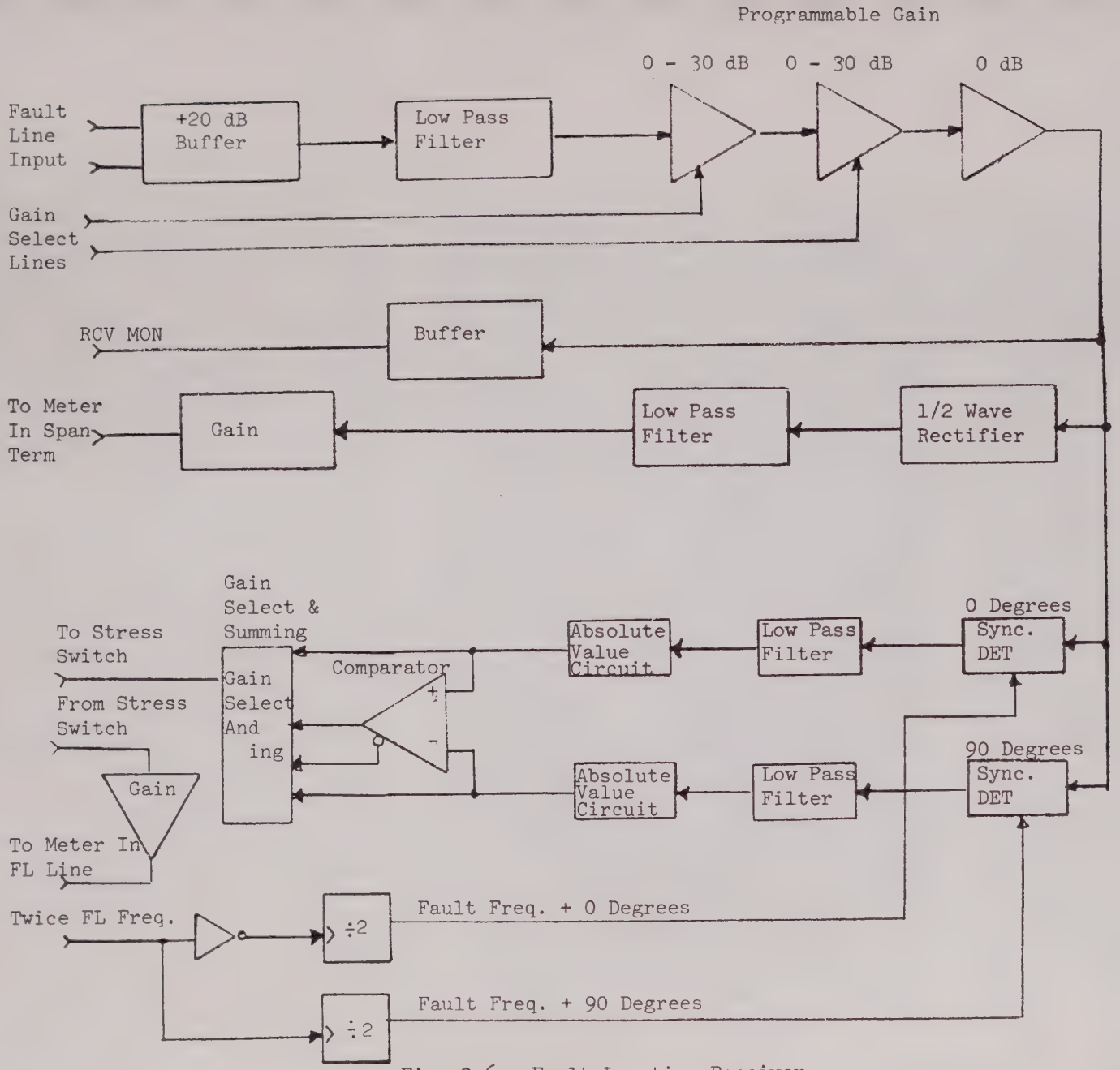



Fig. 3-6: Fault Locating Receiver

3.5.4 Wideband Detection

In Span Term the intent is to measure the wideband (up to 3 kHz) noise present on the fault line. The signal after amplification is directed to a half wave rectifier (U14). This circuit is used to convert the signal to an analogous D.C. level. When the signal is low pass filtered (R12, C23) the D.C. content is equal to the (voltage peak)/Pi. This level is proportional to the noise voltage present. U19-A is used as a gain stage to increase the drive to the meter. Resistor R73 is used as an adjust to set the current drive to the meter.

3.5.5 Fault Locating Detection

In the FL position the intent is to accurately measure the amount of signal in a very narrow bandwidth. This is accomplished using a synchronous detection technique. Depending on the setting of the filter switch, the fault locating signal can be at one of twelve distinct frequencies (See Table 2-1). Depending on the position of the filter switch, a frequency equal to twice the fault locating frequency will be present at Pin N. This signal clocks U2-A directly and is inverted and clocks U2-B. U2 is connected as two divide by two circuits. Since they are clocked by a signal and its complement, the output signals will be 90° out of phase and equal in frequency to the fault locating signal (See Fig. 3-7). The system reset is connected to the circuit's clear inputs so both circuits come up in the same initial states. Since the input is exactly twice the fault signal, the output will be exactly the fault signal frequency. Because of the divide by two circuitry, the two signals would be exactly 90° out of phase except for the gate delay of U3-A, and any difference in the gate delays of U2-A and U2-B. Since the flip-flops are in same package, minimal delay difference exists, but using worse case difference and worse case delay for U3, the amount of difference from 90° would be less than .00001 degrees.

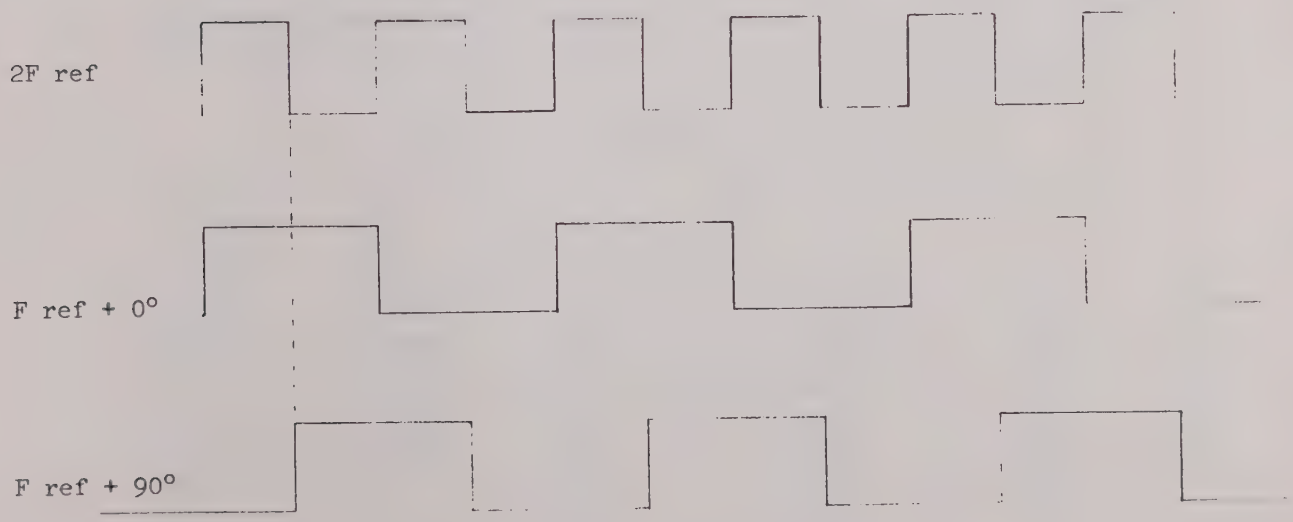



Fig. 3-7: Quadrature Signal Generation

U7 and U9 are op amps connected as synchronous full wave comparators. When the positive inputs of these circuits are grounded, the circuit is a unity gain inverting amplifier. When the positive input is open circuited, the amplifier is a non-inverting unity gain amplifier. The state of the positive inputs is determined by U8, a quad analog switch which is controlled by the two quadrature frequencies generated in U2. The resulting signals are unfiltered, quadrature components of the received FL signal.

3.5.6 Detection Approximation

The signal components at the FL frequency have thus been detected. The amount of D.C. when low pass filtered will be:

$2V_p$ Cos $\theta$ and $2V_p$ Sin $\theta$, where $V_p$ is the peak of the received FL signal and $\theta$ is the phase difference between the transmitted and received FL signals.

U13 is a dual amp which, with the low pass filters (R23, C32 and R54, C47), filters and buffers the outputs. U18 and U17 are dual op-amps which are connected as absolute value circuits. The diodes used are in the closed loop of the amps, thus minimizing the effect of the diode drop.

The remainder of the circuitry is used to implement an algorithm. It is known that given quadrature components $V_p$ Cos $\theta$ and $V_p$ Sin $\theta$ you can obtain $V_p$ by Eqn 3-1. The circuitry needed to implement this equation is not trivial. It requires 2 squaring circuits and

$$\text{Eqn 3-1:} \quad V_p = \sqrt{V_p^2 \cos^2\theta + V_p^2 \sin^2\theta}$$

a square root circuit. It can be shown that the approximation given in Eqn 3-2 is accurate to within .5 dB over all angles. This equation intends to take the absolute value of both, $V_p$ Cos $\theta$ and $V_p$ Sin $\theta$,

$$\text{Eqn 3-2:} \quad V_p = .95 \times \text{larger component} + .46 \times \text{smaller component.}$$

multiply the larger by .95 and the smaller by .46, and add the results together. The amount of error is shown in Table 3-1 for angles up to 45°. The error is cyclic after 45°.

Table 3-1: Approximation Error

| Angle($\theta$) | Cos$\theta$ | Sin$\theta$ | .95xL + .46xS | Error % | Error dB |
|---|---|---|---|---|---|
| 0 | 1.0 | 0 | .95 | -5 | -.44 |
| 4.5 | .997 | .078 | .98 | -2 | -.18 |
| 9.0 | .988 | .156 | 1.01 | +1 | .086 |
| 13.5 | .972 | .233 | 1.03 | +3 | +.26 |
| 18.0 | .951 | .31 | 1.047 | +4.7 | +.40 |
| 22.5 | .923 | .383 | 1.054 | +5.4 | +.46 |
| 27.0 | .891 | .454 | 1.057 | +5.7 | +.48 |
| 31.5 | .853 | .552 | 1.052 | +5.2 | +.44 |
| 36 | .81 | .588 | 1.042 | +4.2 | .36 |
| 40.5 | .76 | .649 | 1.023 | +2.3 | .2 |
| 45.0 | .707 | .707 | 1.0 | 0 | 0 |

U12 is a comparator which determines which signal is larger. The outputs of U12 and its complement are fed to U6. U6 is an analog switch which determines through which resistor the two inputs are fed to U1-A's summing point, thus determining the multiplying factor. U1 has an RC in its feedback loop to minimize the effect of switching transients.

The output of U1 is sent off the board to the STRESS DENSITY switch and depending on the stress density setting, returned through a dividing resistor to R10. This resistor divider drops the level by the same amount the transmitted stress level has been increased. U1-B is a buffer which amplifies the signal to drive the meter. Resistor R72 is used to adjust the current drive to the meter. In series with this resistor is the front panel RECEIVER SENSITIVITY vernier potentiometer. This is used to center the needle if desired.

3.6 A8 Power Supply Board (Schematic 5-10)

The T1D Power board consists of six linear regulators and a simple diode rectifier. The six linear regulators are driven from full wave rectifiers to minimize the amount of peak charge current per cycle. The voltages provided are ± 15V, ± 6.2V, +5V, +5V adj. and +130V.

The ± 6.2V (VR2, VR3) regulators are derived from six volt regulators, whose common terminal is floated slightly above ground. This technique is also used in the 5V adjustable (VR6) regulator. In addition, 2 diodes (CR14, CR15) are used to decrease the minimum output voltage. The 130V output is not regulated since its maximum current draw is only 130 uamps. All the linear regulators have short circuit and thermal overload protection.

3.7 A7 Meter Board (Schematic 5-9)

This board provides connections to the meter pins and houses the ohmmeter circuitry. The FL line pins are connected to the positive input of U1 which has a 10K ohm resistor in series to +5V. Depending on the ratio of the line to 10K ohm, the amp output will vary from 5V ($\infty$) to zero volts (short). The amp output drives the negative meter lead with the positive to +5 volts through R2 and the OHMS ADJUST pot. Switching of the meter for different functions is accomplished by S10 (Refer to Fig. 5-1).

Transformer T1 isolates the FL line from the Fault Locating Receiver.

3.8 A3 Converter Board (Schematic 5-5)

This board converts T1D signals to T1C format and T1C signals to T1D format. The T1C to T1D path of the board begins with an isolation transformer T2 and a bipolar regenerator circuit, IC2, which converts the DS-1C signal at the input to logic levels, D+ and D-, and extracts a synchronous clock C which is buffered in IC3. The data is then encoded into the duobinary format by IC4 using the algorithm that the polarity to be used if there is a one in the next time slot is changed if the current data is a zero, but stays the same if the current data is one. Clocking for the encoded logic functions is provided by the

buffered clock signal. The output of the bipolar to duobinary converter is a logic level representation of the duobinary data signal D2+ and D2-. These two signals are combined in a line driver amplifier IC8 and precisely timed by the clock to produce the three level duobinary signal. A linear output buffer stage provides the output drive capability required. The buffered signal drives the duobinary line through a coupling transformer T4. Integrated circuit IC7 provides a reference voltage which establishes the level of the output signal. The T1D to T1C path of the board begins with an attenuator (R70 - R73) and isolation transformer T1. At the output of the transformer additional loss and signal shaping is provided before the signal is coupled to IC1. Regeneration, clock extraction, and equalization are all accomplished by IC1 and its associated circuitry. The resulting unipolar duobinary signals D1+ and D1- along with the clock C1 are used by the duobinary to bipolar conversion circuit IC5 in developing signals D+ and D-. The positive ones for the outgoing T1C signals are the D+ signal, and the negative ones are the D- signal. Integrated circuit IC6 accepts the "ones" signals and drives the output through transformer T3.

3.9 A2 Artificial Line Board (Schematic 5-4)

This board consists of three balanced circuits providing attenuations of 12 dB, 24 dB, and 24 dB (at 1.576 MHz). The board is used in various series combinations to produce the three losses in repeater testing; short (12 dB), medium (24 dB) and long (48 dB).

# 4.0 MAINTENANCE

## 4.1 Test Equipment Requirements

| | | |
|---|---|---|
| a. | Frequency Counter | GR Model 1191 or equivalent |
| b. | Oscilloscope | Textronix Model 465 or equivalent |
| c. | Oscilloscope Accessories | 2 each X10 Probes and 2 each X1 Probes (calibrate these items to be compatible with the Oscilloscope to be used). |
| d. | Decade Attenuator | General Radio Type 1450-TB or equivalent. |
| e. | Signal Generator | Krohnhite Model 4200 Oscillator or equivalent. |
| f. | Digital Multimeter | Fluke 8000A or equivalent |
| g. | Line Repeaters (Known Good) | Type 258A, Type 281B |
| h. | Office Repeater (Known Good) | 260A Type |
| i. | Power Supply (1 required) | 28V, .5A |
| j. | 3 Loads (See Fig. 4-4, 4-5, 4-2). | |
| k. | 1 Tapped Termination (See Fig. 4-3) | |
| l. | T1C QRSS Generator. (273A) | |
| m. | Resistor 100 ohm, 1%, Alligator Clip at each end. | |
| n. | Resistor 9 meg, Alligator Clip at each end. | |
| o. | One special cable (See Fig. 4-1) | |
| p | Cable BNC to 310 | |
| q. | A, G, M Fault Locating Filters. | |
| r. | HP 400EL AC Voltmeter | |
| s. | 246B extender adapter for repeater. | |
| t. | Scott Random Noise Source Type 811-A | |

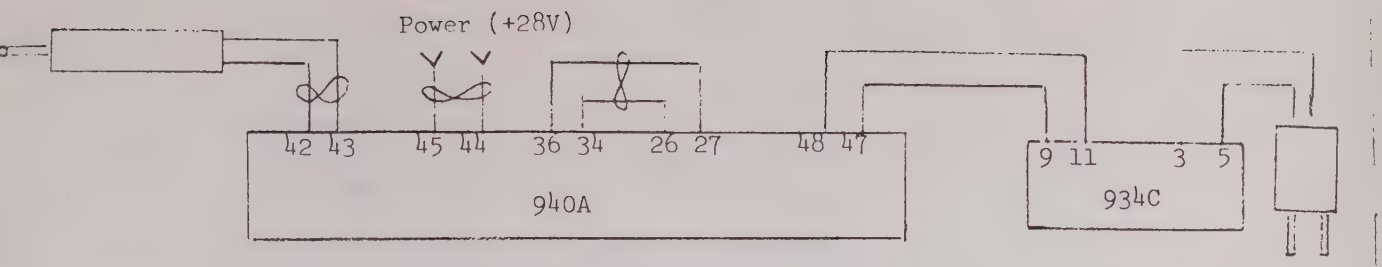



Fig. 4-1: Special Connector

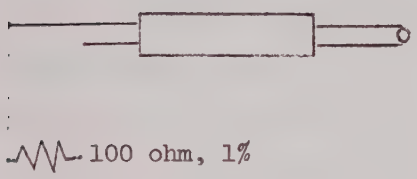
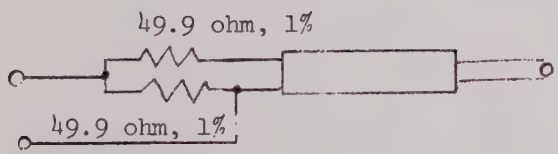



Fig. 4-2 Plug 3




Tapped Termination

Fig. 4-3 Plug 4

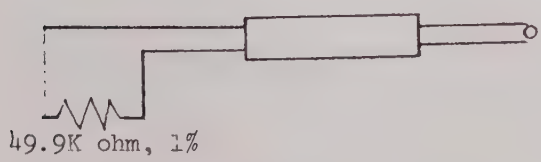



Fig. 4-4 Plug 2

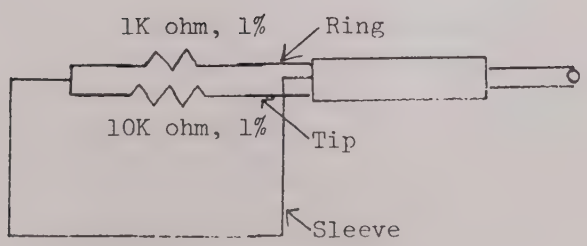



Fig. 4-5 Plug 1

## 4.2 Calibration

### 4.2.1 Preliminary

a. Remove Test Set from its outer case.

CAUTION: Voltages as high as 115 VAC are present in the vicinity of the Power Switch and the Fuseholder.

b. Apply 115 VAC to the Test Set and turn on the Power Switch.

c. Do not connect equipment to the Test Set except as directed below.

### 4.2.2 Oscillator Frequency Adjustment

a. Set FUNCTION Switch to SYS TST 1.

b. Connect Counter to GEN OUT using Plug 4.

c. Set Counter for FREQUENCY measurement with 1 Second counting period.

d. Adjust Capacitor C2 on the A1 board for a frequency of 1,576,000 KHz ± 25 Hz.

e. Set Filter Switch for D. Connect Counter to A1-W.

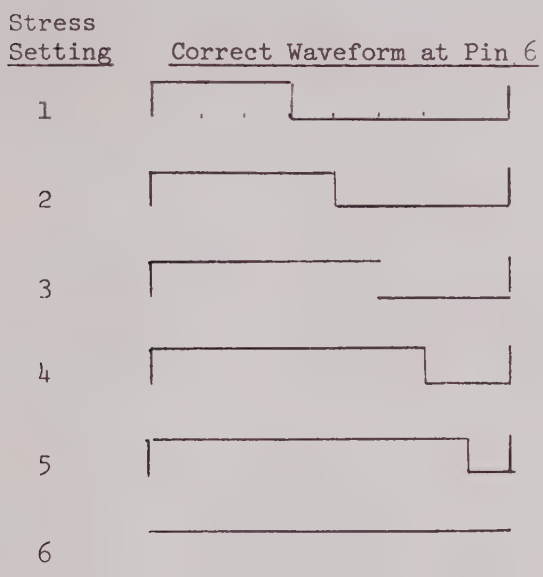
f. Set Counter for PERIOD measurement and 1 ms Time period. Adjust C4 for 414.5077 usec ± .05 usec.

g. With Counter connected to A1-W and FUNCTION Switch in any position except OHMS or SPAN TERM, measure the following frequencies vs. Filter Switch position.

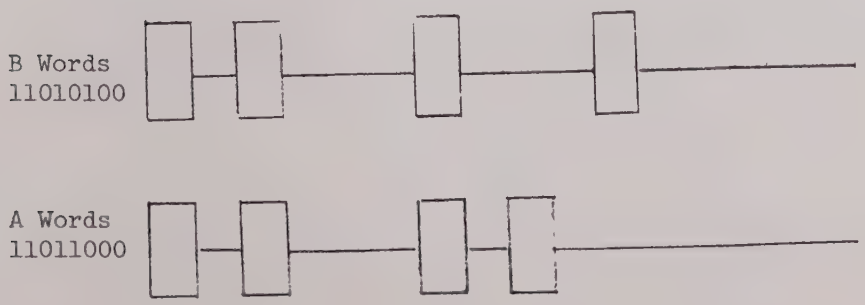
NOTE: Divide frequency by 2 (÷2).

| Filter Switch Position | Frequency @ Pin W (Hz) |
|---|---|
| A | 1664 ± 3.3 |
| B | 1856 ± 3.7 |
| C | 2096 ± 4.2 |
| D | 2412 ± 4.83 |
| E | 2680 ± 5.36 |
| F | 3016 ± 6.03 |
| G | 3444 ± 6.9 |
| H | 4016 ± 8.02 |
| J | 4386 ± 8.77 |
| K | 4826 ± 9.65 |
| L | 5360 ± 10.72 |
| M | 6034 ± 12.06 |

h. With Oscilloscope connected to A1-F, FUNCTION Switch in SYS TST 2, and filter in A, observe the following waveforms vs Stress Setting. Period of waveform is 20.3 usec ± 1%. Use Frequency Counter through Oscilloscope.




j. With scope Channel One connected to A1-G settings as above, trigger scope off Channel One. Connect Channel Two to Tapped Termination in GEN OUT. With scope on A delayed by B, delay rate = 5 usec/Div., and display rate = 1 usec/Div. Scan display for the number of B and A (See Figures) words should be as shown vs. Stress Setting. Position 6 cannot be triggered. Just look for A1-G, and pattern change.



Stress Setting

| | # of Words | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| 1 | B | B | B | A | A | A | A | A |
| 2 | B | B | B | B | A | A | A | A |
| 3 | B | B | B | B | B | A | A | A |
| 4 | B | B | B | B | B | B | A | A |
| 5 | B | B | B | B | B | B | B | A |
| 6 | B | B | B | B | B | B | B | B |

k. Transmitter Output Check

Using Tapped Termination (Plug 4) in GEN OUT the following waveforms should be present.

FUNCTION Position

| | |
|---|---|
| OHMS | No Signal |
| SPAN TERM | No Signal |
| SYS TST 1 | All Ones (3V p-p) |
| SYS TST 2 | Fault Locating Signal (A/B words) (3V p-p) |
| FL | Fault Locating Signal Offset +2.5V (3V p-p) |
| RPT TST 1 | All Ones (3V p-p) |
| RPT TST 2 | All Ones (3V p-p) |
| LEAKAGE | No Signal |

4.2.3 Meter Adjustment

a. Place Function Switch in OHMS position.

b. With no input use mechanical zero to adjust meter for infinite reading.

c. Depress OHMS SHORT and using OHMS ADJUST, adjust meter for zero reading.

4.2.4 Clock Extractor Adjustments

a. Connect T1C QRSS source to DET IN Jack.

| | |
|---|---|
| Oscilloscope | X10 probe to A6-TP3, |
| CH1 | Amplifier 2V/cm |

b. Using a tuning tool, adjust inductor L2 for optimum waveform. The signal should be maximized in amplitude, and there should be minimum spread on waveform (See Fig. 4-6).

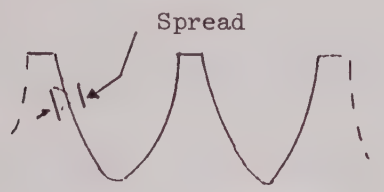



Fig. 4-6: Clock Extractor Adjustment

4.2.4.1 Clock Extractor Phase Adjustment

a. Test equipment adjustments:

| | |
|---|---|
| Oscilloscope | X10 probe connected to A6-TP4, |
| CH1 | Amplifier 2V/cm. |
| CH2 | X10 probe connected to A6-TP1, Amplifier 2V/cm |
| Time Base | Adjust for .1 usec/cm and sync to CH2 |

b. Adjust oscilloscope horizontal position control to set the positive transition of CH1 on the vertical center line.

c. Adjust C27 to position CH2 pulse symmetrically around Center Line (See Fig. 4-7).

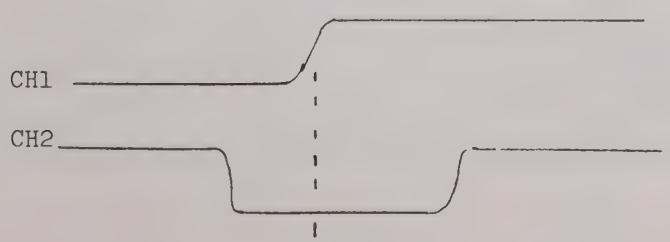



Fig. 4-7: Clock Extractor Phase Adjustment

4.3 Performance Checks

4.3.1 Preliminary
These checks are to be made with specified equipment. They may serve for periodic maintenance, quality control checks, and for post repair checkout. The Test Set must be connected to a power source of 115 VAC ± 10%, 50 to 60 Hz.

4.3.2. Transmitter Checks

4.3.2.1 Transmitter Clock Frequency

a. Allow the Test Set to temperature stabilize by operating for at least one hour at room temperature. The Test Set may be momentarily unplugged only for the purpose of moving it.

b. Connect the Counter input to the GEN OUT jack and the GRD. Use Tapped Termination. Set FUNCTION Switch to SYS TST 1.

c. Adjust the Counter for a one second count interval (to read directly in Hz), and set the Counter's input control for a consistent display. The Counter should register between 1,575,975 and 1,576,025 at the end of each count interval.

d. Disconnect the Counter.

4.3.2.2 Bipolar Output (T1C)

a. Set FUNCTION Switch to SYS TST 1, and insert the Tapped Termination into GEN OUT.

b. Adjust the Oscilloscope for 0.5V/cm and .05us/cm.

c. The measurements designated 1 and 2 in Fig. 4-8 should be between 2.7 and 3.3 cm (1.35 and 1.65 volts). Measurements 1 and 2 should differ by not more than 0.15 cm (0.775 volts)

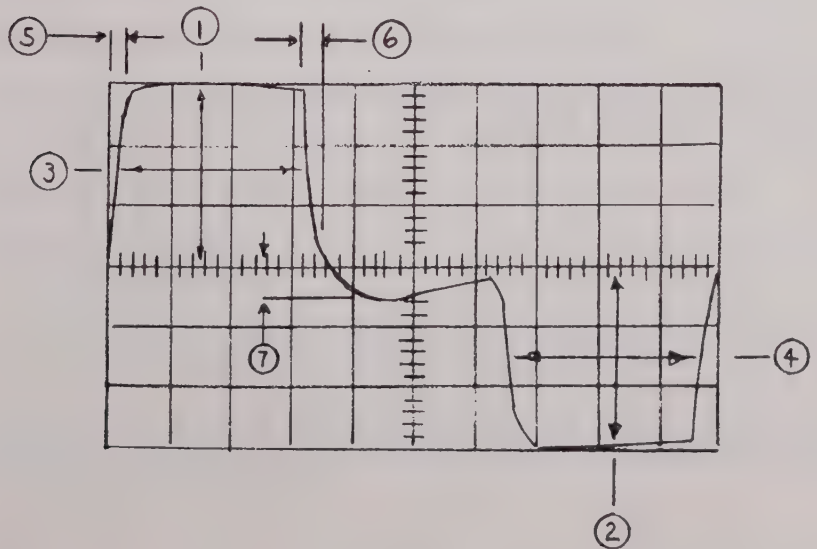



Fig. 4-8: Bipolar Waveform

d. Measurements 3 and 4 should be between 2.9 cm and 3.5 (145 and 175 nsec). These measurements should not idffer by more than .3 cm (15 nsec).

e. Measurements 5 and 6 taken between 20% and 80% should be less than 1.0 cm (50 nsec).

f. Measurement 7 should not exceed 10% of the peak amplitude .3 cm. CAUTION: Poor Probe grounding will greatly affect this measurement.

g. Peak to peak base line noise less than 10% of peak amplitude.

h. Fall time (6) 20% to 80% max. amplitude should be less than 70 nsec.

4.3.2.3 Ohmmeter

a. Set FUNCTION Switch to OHMS. Using Plug (Fig.4-3) in GEN OUT - verify no signal present.

b. With no input, set mechanical adjust for $\infty$ reading on ohms scale.

c. Press OHMS SHORT and use OHMS ZERO to adjust meter to read zero.

d. Place Plug (Fig. 4-5) in FL LINE Jack.

e. Put OHMMETER Switch to TIP-GND. Meter should read 10K Ohms $\pm$ 5%.

f. Put OHMMETER Switch to RING-GND. Meter should read 1K Ohms $\pm$ 5%.

g. Connect Plug (Fig. 4-4) to FL Jack. Set OHMMETER to TIP-RING. Ohmmeter should read 50K $\pm$ 5%.

4.3.2.4 SPAN TERM

a. Hook up test equipment as shown in Fig. 4-9.

b. Set signal source for 1.5 KHz $\pm$ 5%.

c. Place FUNCTION Switch in SPAN TERM position.

d. With Plug 3 in GEN OUT verify no signal present with oscilloscope. Set attenuator to 0 dB, and set RECEIVER SENSITIVITY to 0 dBm.

e. Measure input to set. Adjust to 0.754 Vrms $\pm$ 10 mV.

f. Meter reading should be -2 dB $\pm$ 1 dB. (Adjust R73 on A5 from nominal if required).

g. Increase decade box attenuator by 10 dB, and RECEIVER SENSITIVITY by -10 dB. Readings should stay constant within $\pm$ 1 dB.

h. Repeat Step g until RECEIVER SENSITIVITY is in -80 dB position. Accuracy is $\pm$ 3 dB in 80 - 90 dB position. Continue attenuating until -92 dBm is reached.

4.3.2.6 SYS TST 2

a. Set FUNCTION Switch to SYS TST 2. Hook oscilloscope Channel 1 to board A6 Pins R and S.

b. Set STRESS DENSITY Switch to Position 1, and FILTER SWITCH to Position G.

c. Connect Channel Two of scope to transmitter board Pin F. Set scope for ALT and trigger off Channel Two.

d. Waveform should be as shown in Section 4.1.2(j). (3 B words (11010100) and 5 A words (11011000).

e. Moving to the next highest stress level, the number of B words should increase by one.

f. Repeat Step e until completion of stress level 6. (Position 6 cannot be triggered. Look for change in pattern).

4.3.2.7 F.L.

a. Set FUNCTION Switch to FL position; STRESS DENSITY on 1; FILTER Switch to A, and RECEIVER SENSITIVITY = 0 dBm.

b. Hook up circuitry as shown in Fig. 4-10.

c. Adjust vernier on the test set full clockwise (CAL).

d. Set attenuator for -40 dB and adjust vernier for -2 dB on test set meter. Voltage on AC Voltmeter should read 7.54 mV $\pm$ 10%. (Adjust R72A on A5 as required).

e. Turn vernier full counter clockwise. Meter should read -10 dB to -16 dB.

f. Reset vernier on the test set.

g. Set STRESS DENSITY to next highest stress level, allow meter time to respond, meter should read the same $\pm$ 1 dB.

h. Repeat for all stress levels up to and including six.

i. Reset STRESS DENSITY to 4.

j. Increase attenuator setting by 10 dB, increase RECEIVER SENSITIVITY by -10 dB, reading should remain constant within $\pm$ 1 dB.

k. Repeat Step j until RECEIVER SENSITIVITY reads -100 dB.

l. Reset attenuator for 0 dB, and RECEIVER SENSITIVITY for -40 dB. Turn to adjacent Filters. Reading should drop off scale.

m. Set STRESS DENSITY for Position 1. Repeat Step d and l for Filter Frequencies G and M, using corresponding Fault Locating Filter.

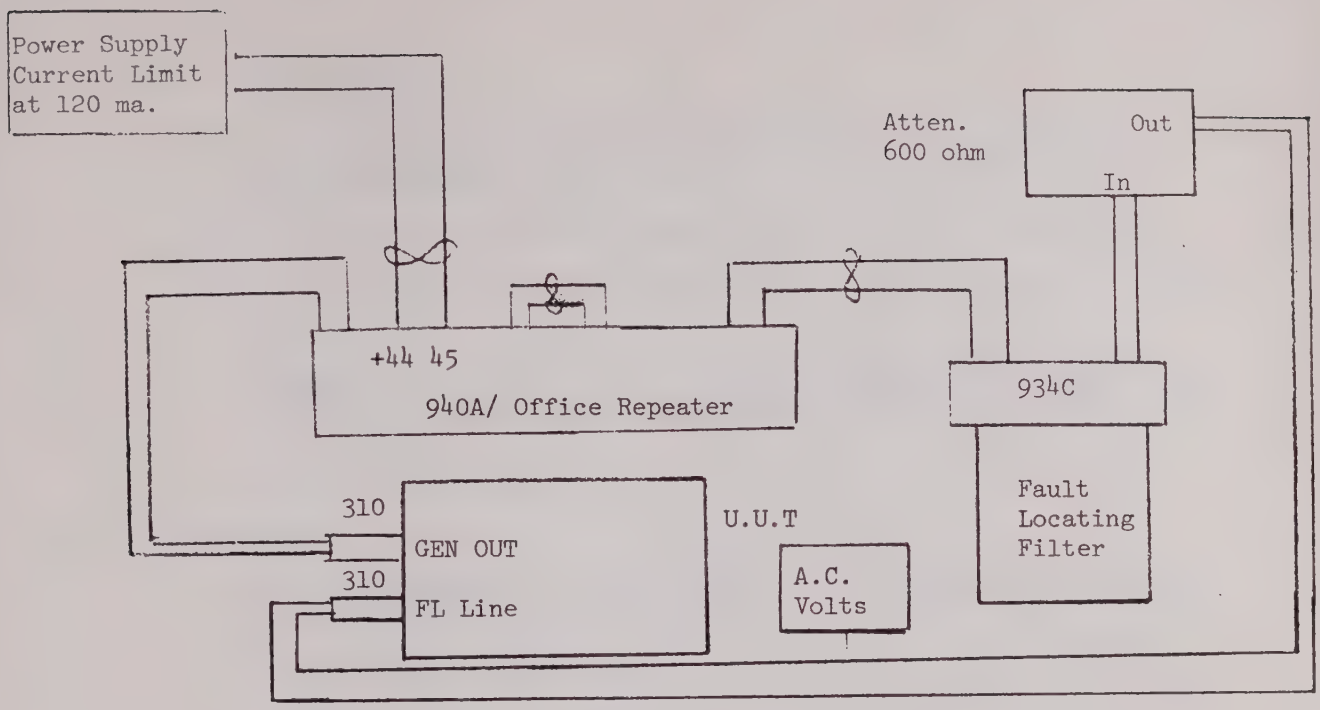



Fig. 4-10: Fault Locate Test Arrangement

n. Using A Filter connect Random Noise Generator to output of attenuator through 910 ohm resistor.

o. Set STRESS DENSITY to Level 1 and FILTER Switch in Position A.

p. Connect Noise Source to attenuator output through 910 ohm resistor.

q. Turn Noise Source on, but to minimum level. Set Noise Type Switch to AF (audio frequencies).

r. With RECEIVER SENSITIVITY Switch in -40 dB position and vernier fully clockwise, adjust attenuator until test set meter indicates -5 dB.

s. Turn FUNCTION Switch to SPAN TERM, and RECEIVER SENSITIVITY to -30 dB.

t. Adjust Noise Source until meter indicates -5 dB.

u. Turn FUNCTION Switch to FL and RECEIVER SENSITIVITY to -40 dB.

v. Meter should read -5 dB. Meter waver should be approximately $\pm$ 1 dB or less with an allowable random spike.

4.3.2.8 T1C Receiver Testing

a. Connect the GEN OUT jack to DS1C DET IN using a patch cable. Set FUNCTION Switch to SYS TST 1.

b. The PULSES and SYS TST 1 lights should be on, all others off.

c. Using a 273A, connect the 273A output to DS1C DET IN jack. PULSES should light.

d. Manually insert B.P.V.s with the 273A INSERT ERRORS switch. The VIOLATIONS light should blink, PULSES light should be on.

e. Disconnect the 273A.

4.3.2.9 Meter Testing

a. Set FUNCTION Switch to RPTS TST 1, and REPEATER POWER Switch to A, and MILLIAMPS/VOLTS to MILLIAMPS.

b. Turn CURRENT ADJUST Switch fully counter clockwise.

c. Connect 100 ohm, 1/4W, 1% resistor with alligator clips from A4-H to A4-N.

d. Connect Voltmeter across resistor (meter must be floated).

e. Increase current adjust until the test set meter reads 75 ma.

f. Meter should read 7.5V ± 3% (adjust A4-R10 as required).

g. Increase current adjust until T1D reads 100 ma. Voltmeter should read 10V ± 3%.

h. Remove voltmeter.

i. Turn Current Adjust until meter reads 100 ma.

j. Turn MILLIAMPS/VOLTS to VOLTS. Meter should read 10V ± 6%.

k. Adjust Current Adjust until voltage = 12V. Turn MILLIAMPS/VOLTS to MILLIAMPS. Meter should read 120 ma ± 6%.

l. Turn Current Adjust to 150 ma.

m. Switch MILLIAMPS/VOLTS to VOLTS. Meter should read 15V ± 6%. Remove the resistor.

4.3.2.10 Repeater Testing

a. Set FUNCTION Switch to RPTR TST 1, ART LINE to SHORT, REPEATER TEST Switch to UNI-DIR SIDE 2 and REPEATER POWER to A.

b. Set MILLIAMPS/VOLTS Switch to MILLIAMPS and Current Adjust full counter clockwise.

c. Insert known good 258A type Repeater in 258A slot.

d. Turn Current Adjust up until meter reads approximately 120 ma.

e. Set MILLIAMPS/VOLTS Switch to VOLTS. Meter should read approximately 12.5 Volts D.C.

f. Set REPEATER TEST to SIDE 2 and FUNCTION to RPTR TST 1.

g. Set ART LINE to SHORT. The PULSES, SYS TST 1, and FL ABSENCE lights should be on.

h. Switch ART LINE to LONG. The PULSES, SYS TST 1, and FL ABSENCE lights should be on.

i. Set REPEATER TEST to UNI-DIR SIDE 1. Repeat Steps g and h.

j. Set FUNCTION Switch to RPTR TST 2. Repeat Steps g - i. This time the lights on should be PULSES and SYS TST 1.

k. Change REPEATER TEST Switch to BI-DIR SIDE 1, FUNCTION to RPTR TST 1. Repeat Steps g, h, and i using 281B repeater and adapter.

l. Set REPEATER POWER to B. Same lights should be on.

4.3.2.11 LEAKAGE

a. Insert 258A Line Repeater. Set FUNCTION Switch to LEAKAGE.

b. LEAKAGE indicator light should remain off.

c. Remove Repeater, LEAKAGE light should come on.

d. Remove Repeater, turn set off. Attach 9 megohm resistor from A4-E to case (GND).

e. Turn set on, LEAKAGE LED should light.

4.3.2.12 Office Repeater

a. Set REPEATER TEST to OFFICE. Insert known good office repeater. Check meter in milliamp position, set to 120 ma. Check meter in volts position, should read approximately 23 volts.

b. Set FUNCTION Switch to RPTR TST 1, ART LINE to SHORT.

c. Only PULSES, SYS TST 1 and FL ABSENCE lights should be on.

d. Set ART LINE to MED., only PULSES, SYS TST 1, and FL ABSENCE lights should be on.

e. Set ART LINE to LONG, all lights except FL ABSENCE should be out.

f. Set FUNCTION Switch to RPTR TST 2, ART LINE to SHORT. Repeat Steps c and d. This time only PULSES and SYS TST 1 lights should be on.

## DIAGRAMS

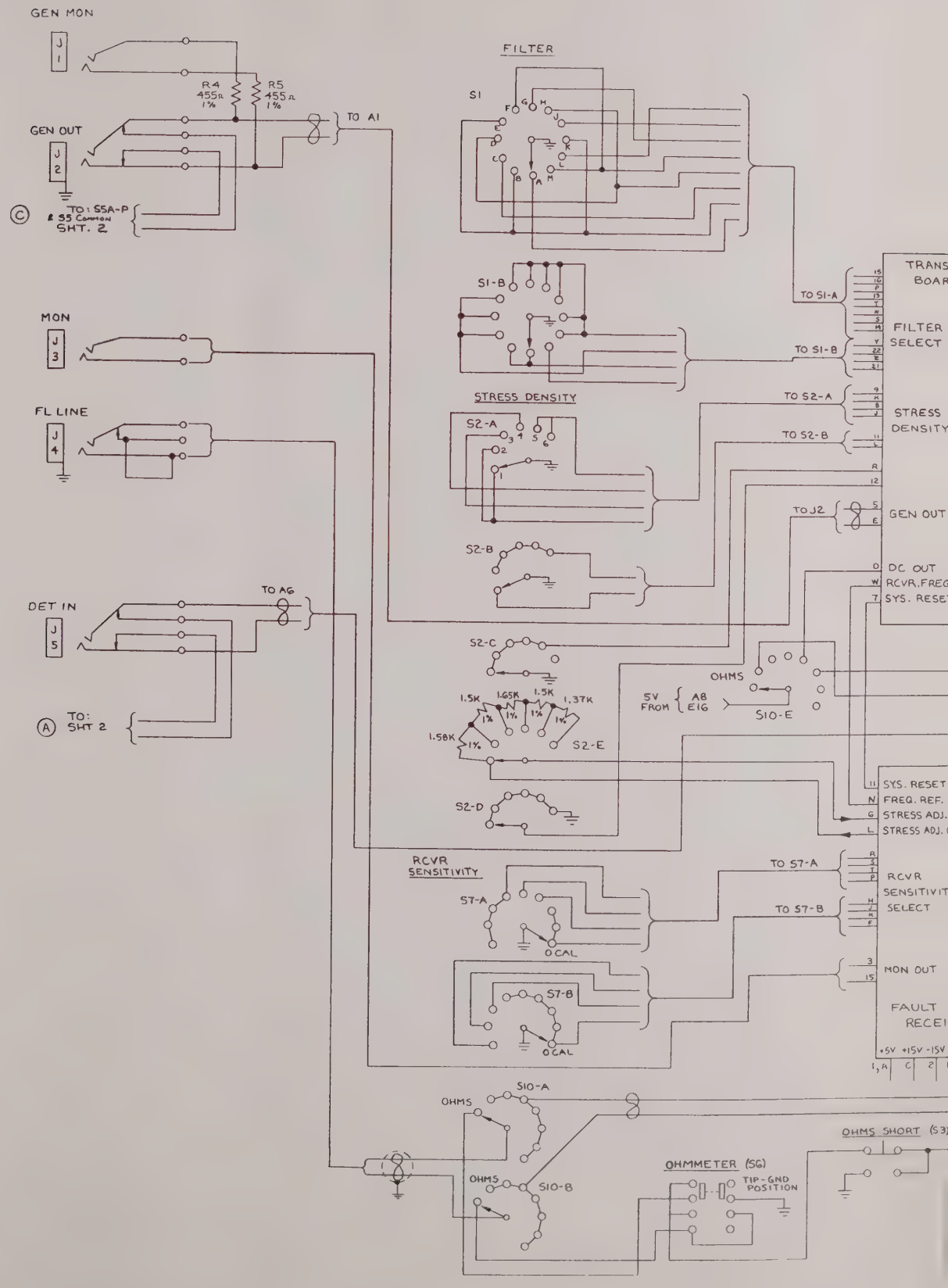

Fig. 5-1 T1D Interconnect Schematic (Sheet 1) - T1D-110
Fig. 5-2 T1D Interconnect Schematic (Sheet 2) - T1D-110

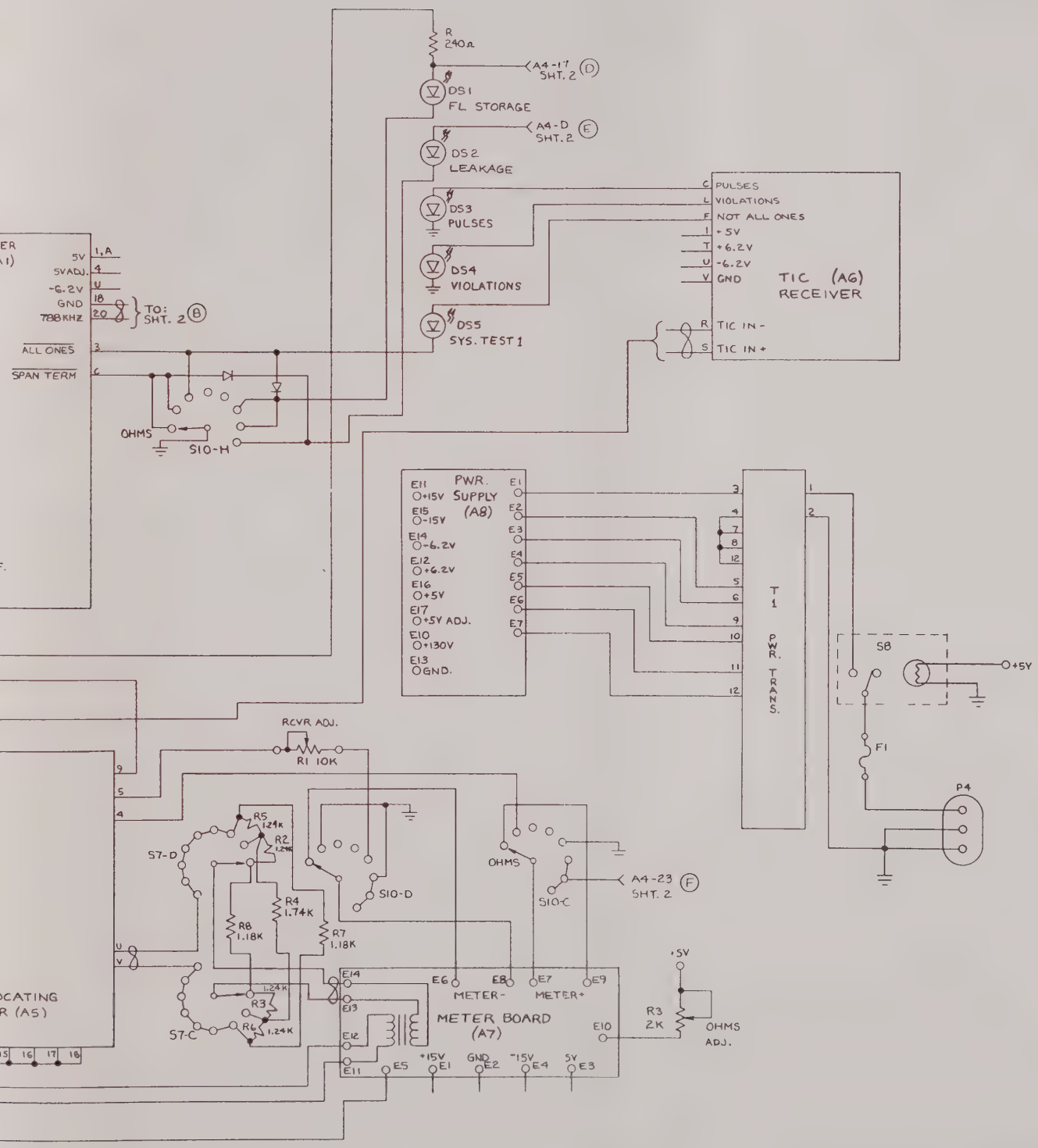
Fig. 5-3 Transmitter Board (A1) Schematic - T1D-103
Fig. 5-4 Artificial Line Board (A2) Schematic - T1D-105
Fig. 5-5 T1C/T1D T1D/T1C Converter Board (A3) Schematic - T1D-106
Fig. 5-6 Repeater Interface Board (A4) Schematic - T1D-102
Fig. 5-7 Fault Locating Receiver (A5) Schematic - T1D-101
Fig. 5-8 DET IN Receiver (A6) Schematic - T1D-104
Fig. 5-9 Meter Interface Board (A7) Schematic - T1D-107
Fig. 5-10 Power Supply (A8) Schematic - T1D-109

Fig. 5-11 Transmitter Board (A1) Assembly Drawing - T1D-203
Fig. 5-12 Artificial Line Board (A2) Assembly Drawing - T1D-205
Fig. 5-13 T1C/T1D T1D/T1C Converter Board (A3) Assembly Drawing - T1D-206
Fig. 5-14 Repeater Interface Board (A4) Assembly Drawing - T1D-202
Fig. 5-15 Fault Locating Receiver (A5) Assembly Drawing - T1D-201
Fig. 5-16 DET IN Receiver (A6) Assembly Drawing - T1D-204
Fig. 5-17 Meter Interface Board (A7) Assembly Drawing - T1D-207
Fig. 5-18 Power Supply Board (A8) Assembly Drawing - T1D-209

Fig. 5-19 Transmitter Board (A1) Circuit Pattern (Component Side) - PMT1D-403
Fig. 5-20 Transmitter Board (A1) Circuit Pattern (Non-Component Side) - PMT1D-403
Fig. 5-21 Artificial Line Board (A2) Circuit Pattern (Non-Component Side)- PMT1D-405
Fig. 5-22 T1C/T1D T1D/T1C Converter Board (A3) Circuit Pattern (Component Side) - PMT1D-406
Fig. 5-23 T1C/T1D T1D/T1C Converter Board (A3) Circuit Pattern (Non-Component Side) - PMT1D-406
Fig. 5-24 Repeater Interface Board (A4) Circuit Pattern (Component Side) - PMT1D-402
Fig. 5-25 Repeater Interface Board (A4) Circuit Pattern (Non-Component Side) - PMT1D-402
Fig. 5-26 Fault Locating Receiver Board (A5) Circuit Pattern (Component Side) - PMT1D-401
Fig. 5-27 Fault Locating Receiver Board (A5) Circuit Pattern (Non-Component Side) - PMT1D-401
Fig. 5-28 DET IN Receiver Board (A6) Circuit Pattern (Component Side) - PMT1D-404
Fig. 5-29 DET IN Receiver Board (A6) Circuit Pattern (Non-Component Side) - PMT1D-404
Fig. 5-30 Meter Interface Board (A7) Circuit Pattern (Non-Component Side) - PMT1D-407
Fig. 5-31 Power Supply Board (A8) Circuit Pattern (Component Side) - PMT1D-409
Fig. 5-32 Power Supply Board (A8) Circuit Pattern (Non-Component Side) - PMT1D-409

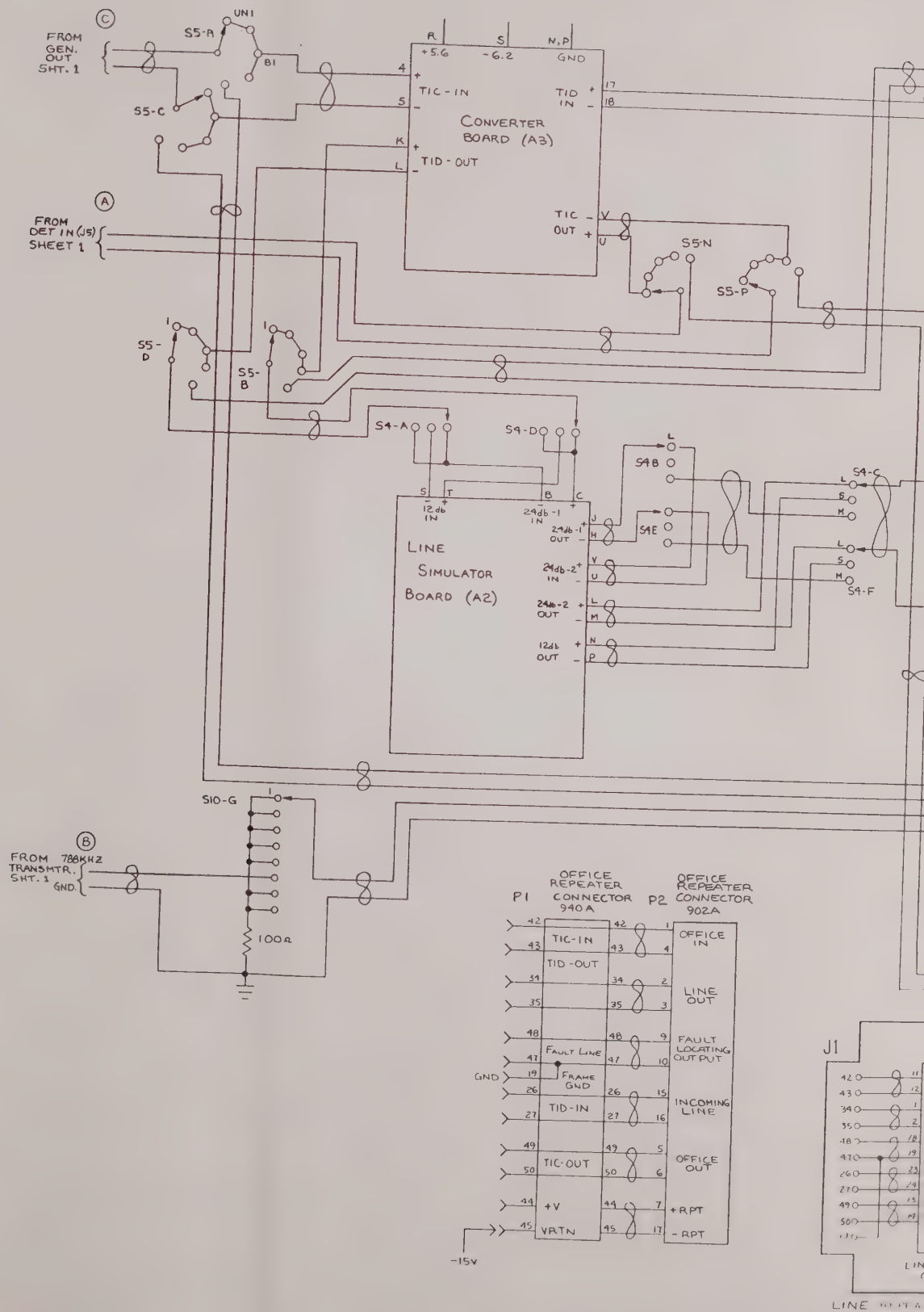
Fig. 5-33 Transmitter Board (A1) Schematic - T1D-103 (Early models)

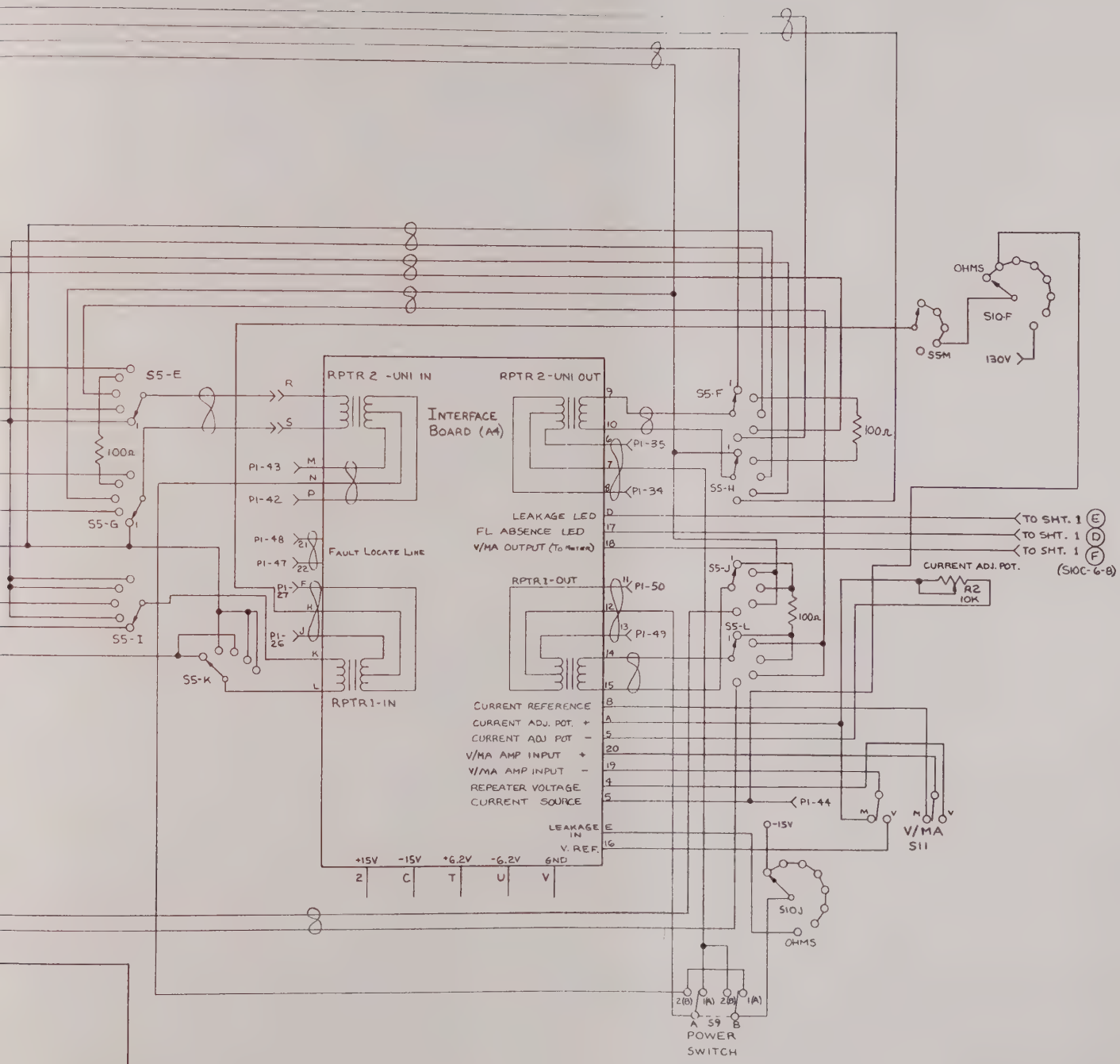

GEN MON
J1
R4 455Ω 1%
R5 455Ω 1%
TO A1
GEN OUT
J2
TO: SSA-P & 55 Common SHT. 2
MON
J3
FL LINE
J4
DET IN
J5
TO AG
TO: SHT 2
FILTER
S1
S1-B
TO S1-A
TO S1-B
FILTER SELECT
STRESS DENSITY
S2-A
S2-B
TO S2-A
TO S2-B
STRESS DENSITY
TO J2
GEN OUT
DC OUT
RCVR.FREQ
SYS. RESET
S2-C
OHMS
5V FROM A8 E16
S10-E
1.5K 1% 1.65K 1% 1.5K 1% 1.37K 1% 1.58K 1%
S2-E
S2-D
SYS. RESET
FREQ. REF.
STRESS ADJ.
STRESS ADJ.
RCVR SENSITIVITY
S7-A
TO S7-A
TO S7-B
RCVR SENSITIVITY SELECT
0 CAL
S7-B
0 CAL
MON OUT
FAULT RECEI
+5V +15V -15V
S10-A
OHMS
OHMS
S10-B
OHMMETER (S6)
TIP-GND POSITION
OHMS SHORT (S3)




T1D Interconnect Schematic
(Sheet 1)
T1D-110

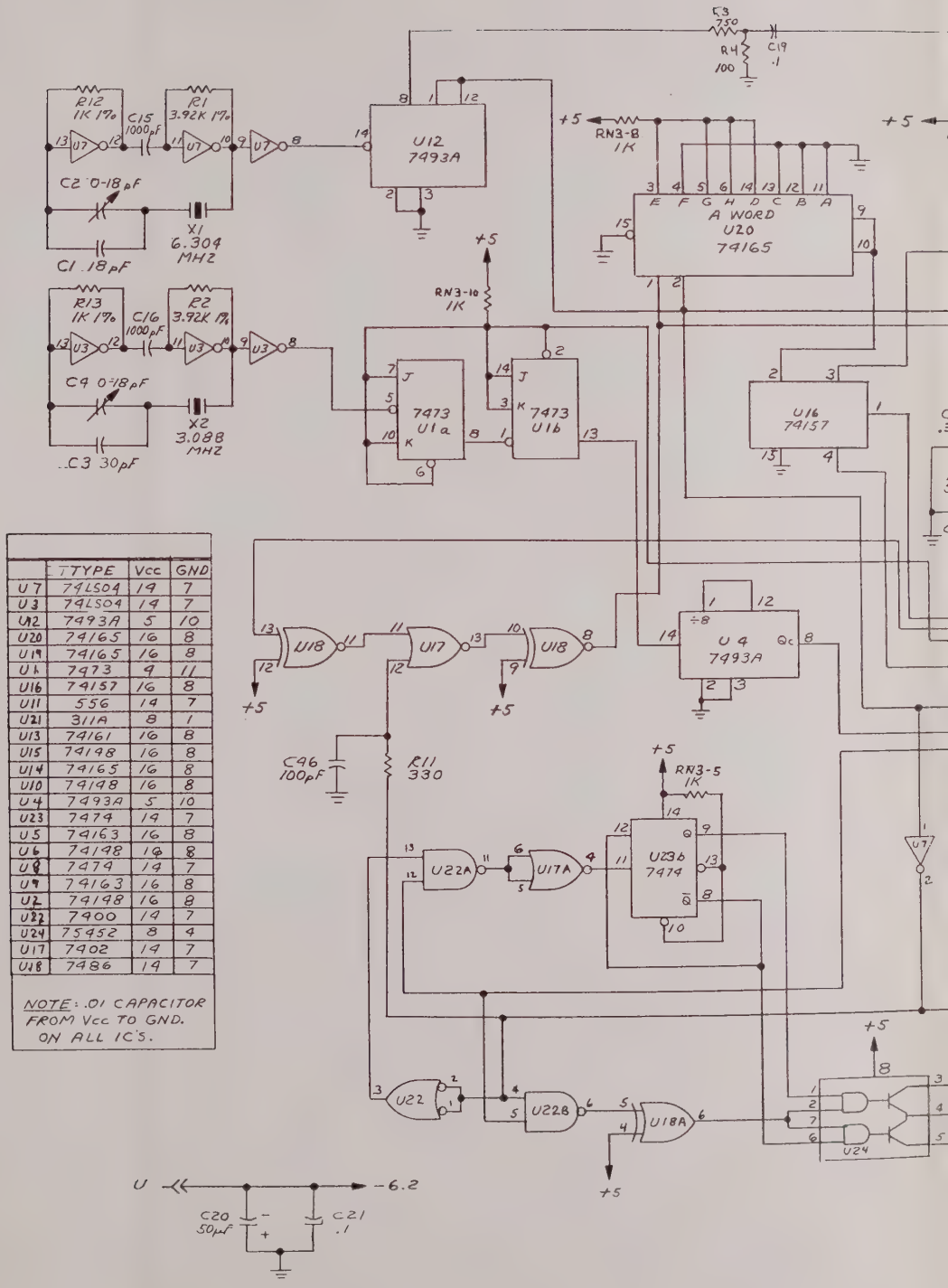
Fig. 5-1


FROM GEN. OUT SHT. 1
FROM DET IN (J5) SHEET 1
FROM 788KHZ TRANSMTR. SHT. 1
GND.
S5-A
S5-C
S5-D
S5-B
S5-N
S5-P
S9-A
S9-D
S9-B
S9-E
S9-C
S9-F
S10-G
100Ω
CONVERTER BOARD (A3)
TIC-IN
TID-OUT
TID IN
TIC OUT
+5.6
-6.2
GND
LINE SIMULATOR BOARD (A2)
12db IN
29db-1 IN
29db-1 OUT
29db-2 IN
29db-2 OUT
12db OUT
P1 OFFICE REPEATER CONNECTOR 940A
P2 OFFICE REPEATER CONNECTOR 902A
TIC-IN
TID-OUT
FAULT LINE
FRAME GND
TID-IN
TIC-OUT
+V
VRTN
OFFICE IN
LINE OUT
FAULT LOCATING OUTPUT
INCOMING LINE
OFFICE OUT
+RPT
-RPT
-15V
J1



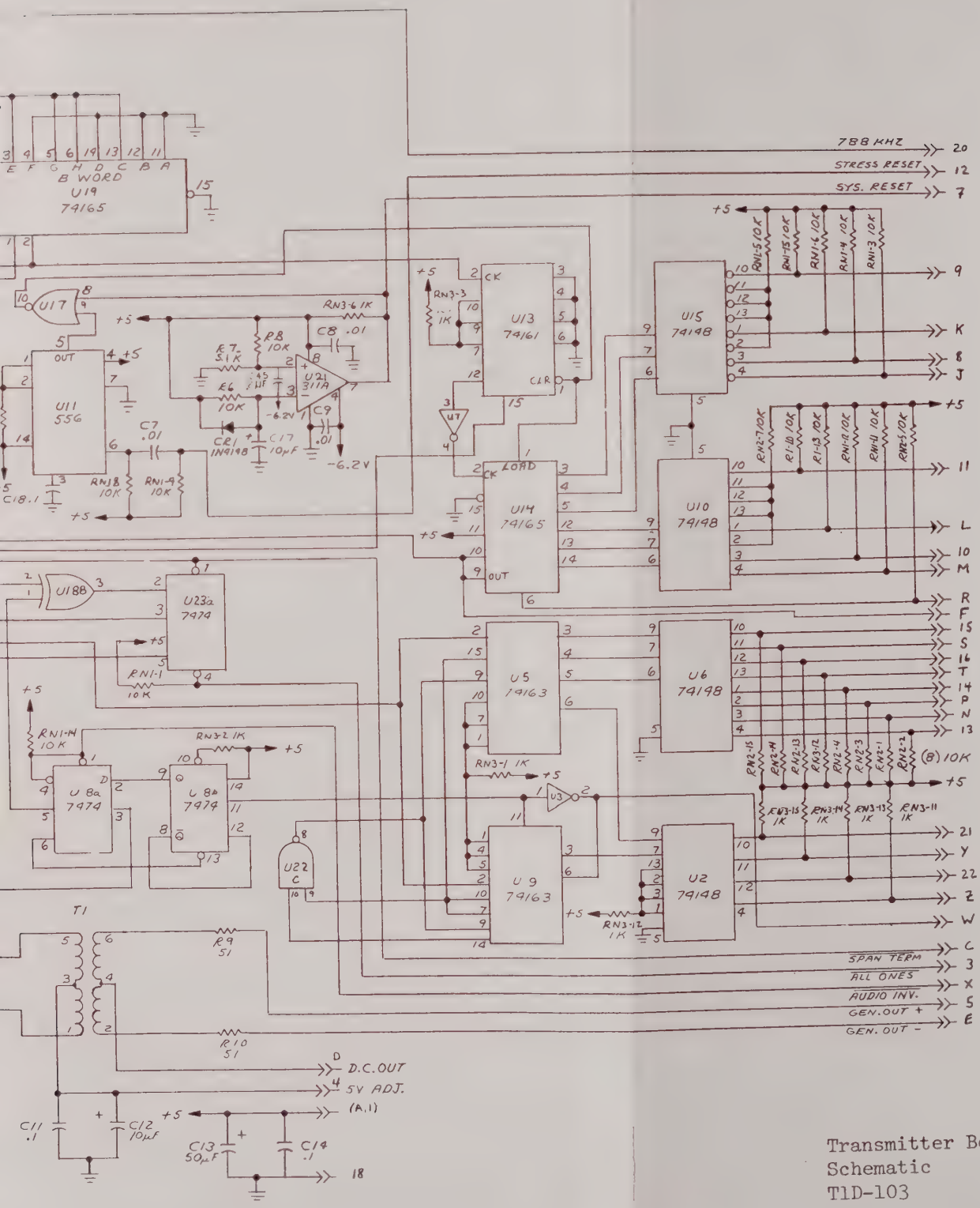

T1D Interconnect Schematic
(Sheet 2)
T1D-110

Fig. 5-2



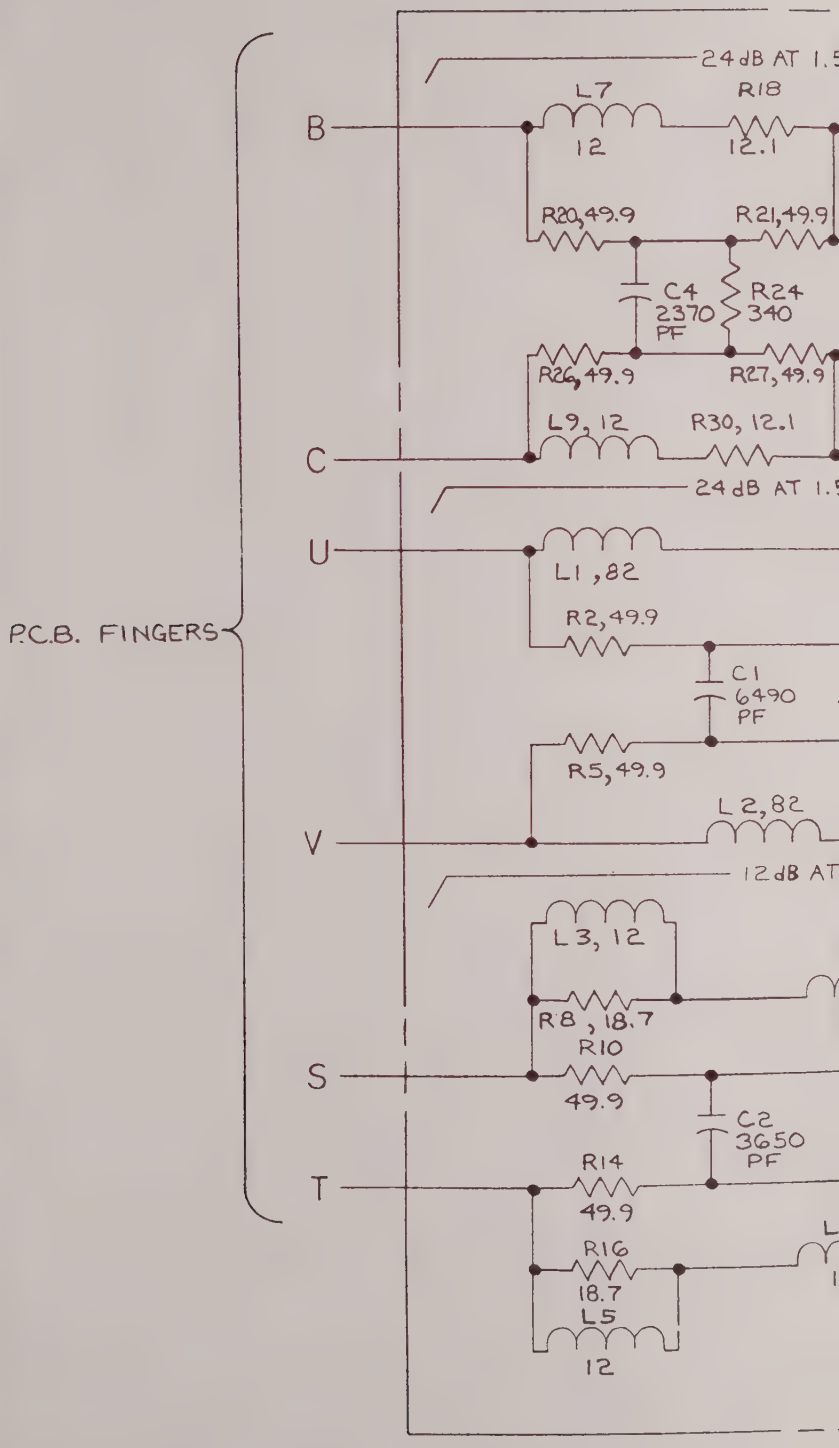

| | TYPE | Vcc | GND |
|---|---|---|---|
| U7 | 74LS04 | 14 | 7 |
| U3 | 74LS04 | 14 | 7 |
| U12 | 7493A | 5 | 10 |
| U20 | 74165 | 16 | 8 |
| U19 | 74165 | 16 | 8 |
| U1 | 7473 | 9 | 11 |
| U16 | 74157 | 16 | 8 |
| U11 | 556 | 14 | 7 |
| U21 | 311A | 8 | 1 |
| U13 | 74161 | 16 | 8 |
| U15 | 74198 | 16 | 8 |
| U14 | 74165 | 16 | 8 |
| U10 | 74198 | 16 | 8 |
| U4 | 7493A | 5 | 10 |
| U23 | 7474 | 14 | 7 |
| U5 | 74163 | 16 | 8 |
| U6 | 74198 | 16 | 8 |
| U8 | 7474 | 14 | 7 |
| U9 | 74163 | 16 | 8 |
| U2 | 74198 | 16 | 8 |
| U22 | 7400 | 14 | 7 |
| U24 | 75452 | 8 | 4 |
| U17 | 7402 | 14 | 7 |
| U18 | 7486 | 14 | 7 |

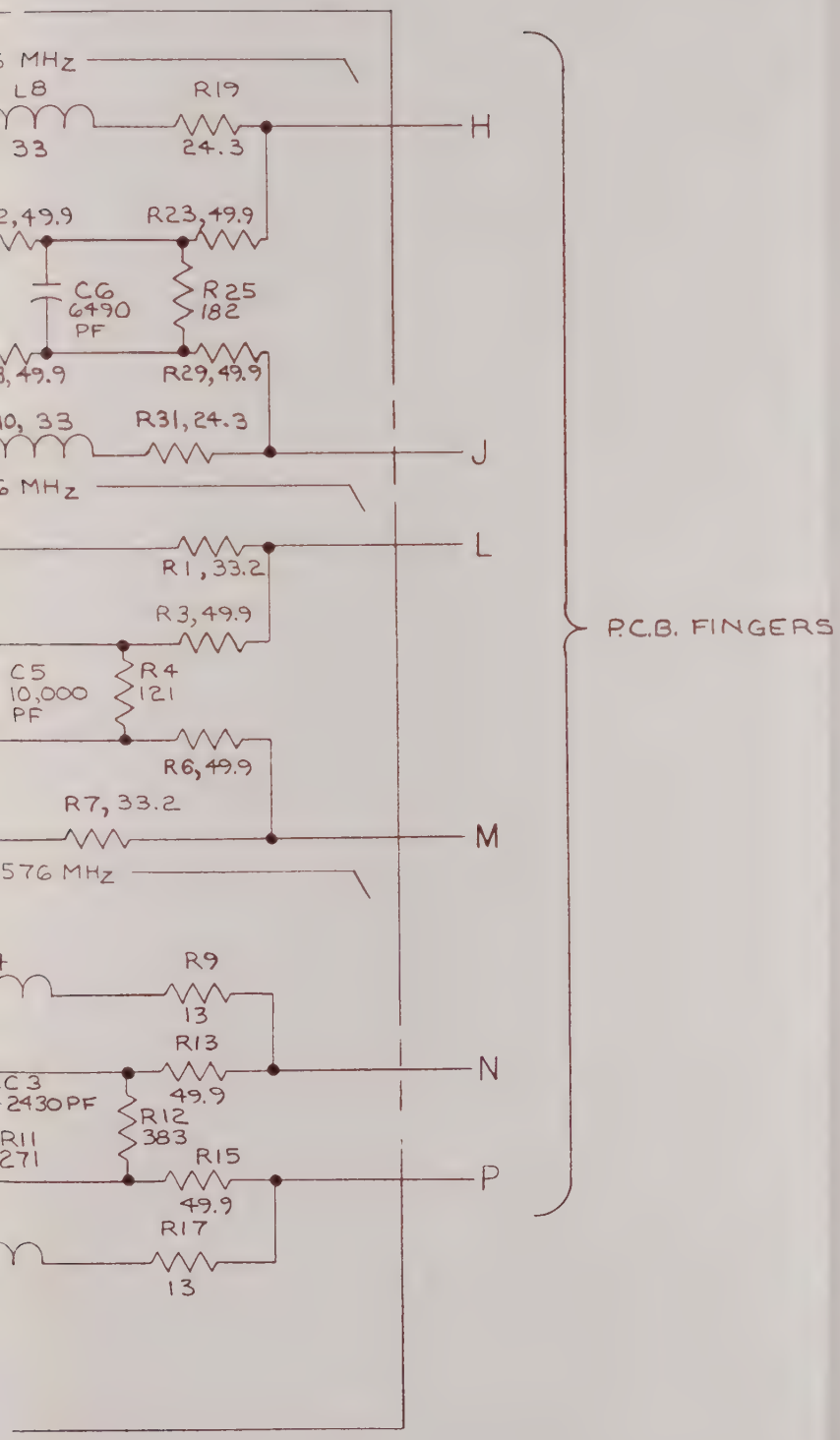
NOTE: .01 CAPACITOR FROM Vcc TO GND. ON ALL IC'S.




Transmitter Board (A1)
Schematic
T1D-103

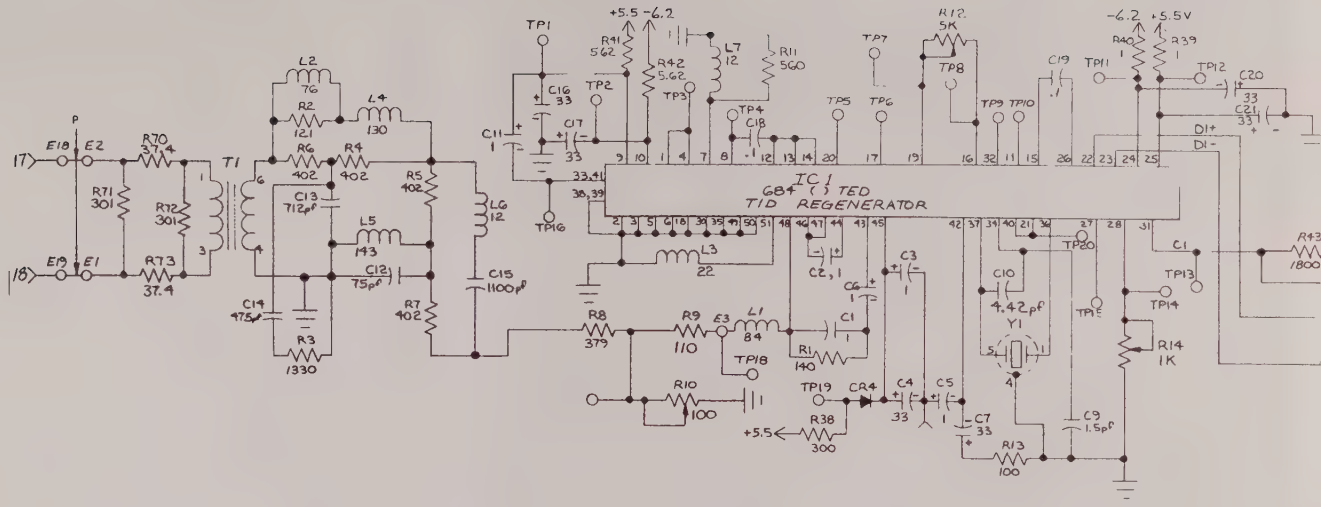
Fig. 5-3

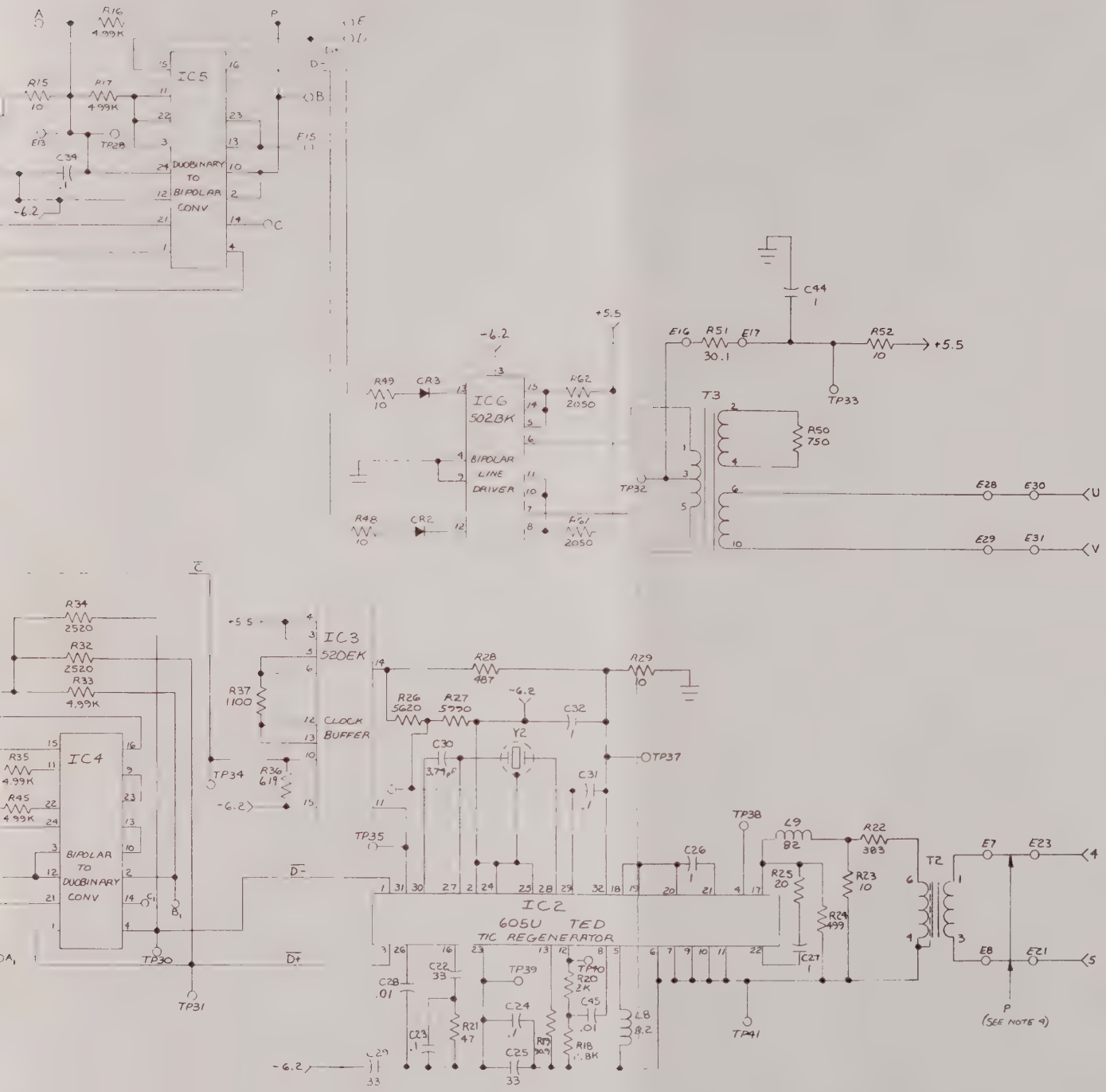

P.C.B. FINGERS
B
C
U
V
S
T
24 dB AT 1.5
L7
12
R18
12.1
R20, 49.9
R21, 49.9
C4
2370
PF
R24
340
R26, 49.9
R27, 49.9
L9, 12
R30, 12.1
24 dB AT 1.5
L1, 82
R2, 49.9
C1
6490
PF
R5, 49.9
L2, 82
12 dB AT
L3, 12
R8, 18.7
R10
49.9
C2
3650
PF
R14
49.9
R16
18.7
L5
12




Artificial Line Board (A2)
Schematic
T1D-105

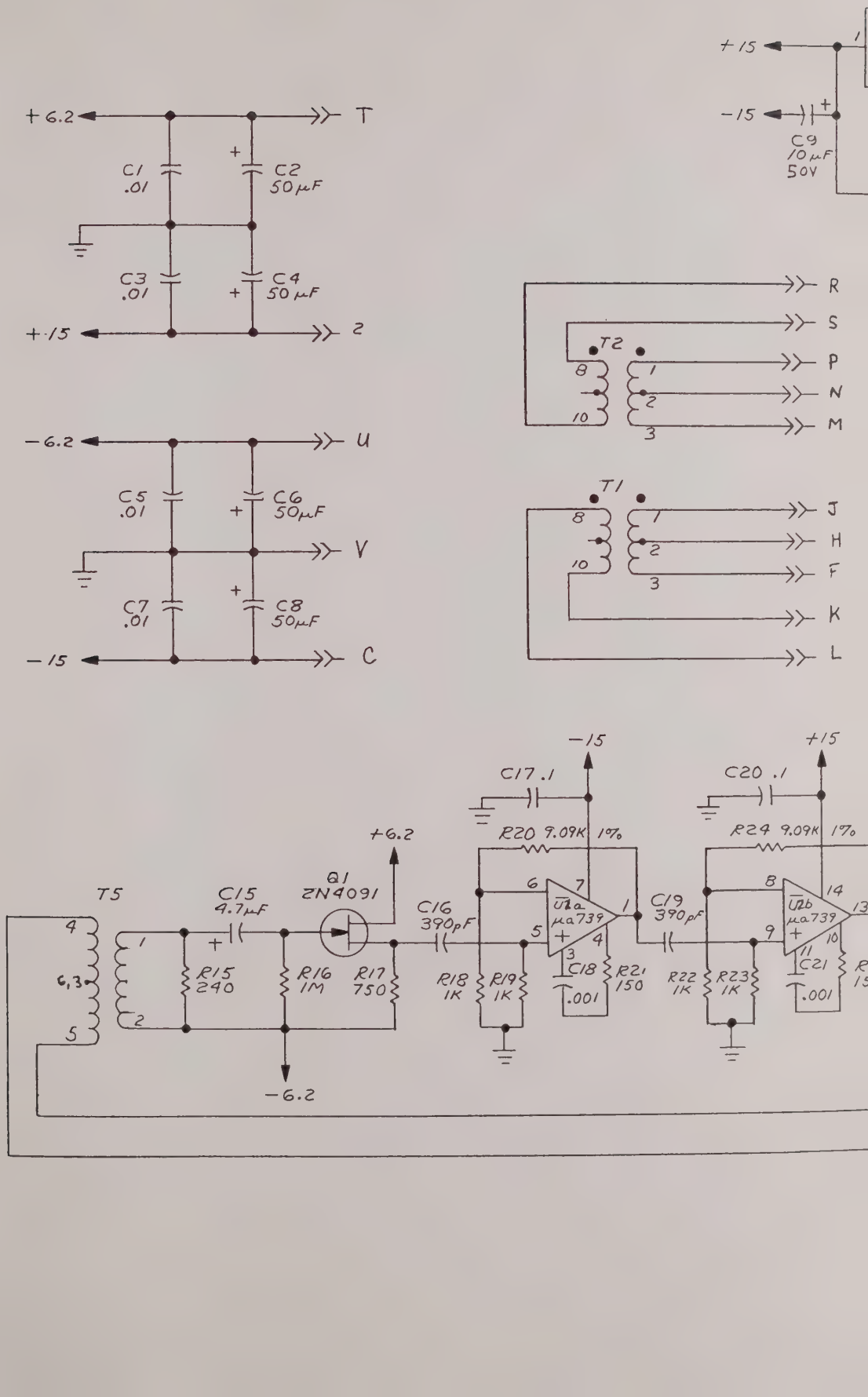
Fig. 5-4

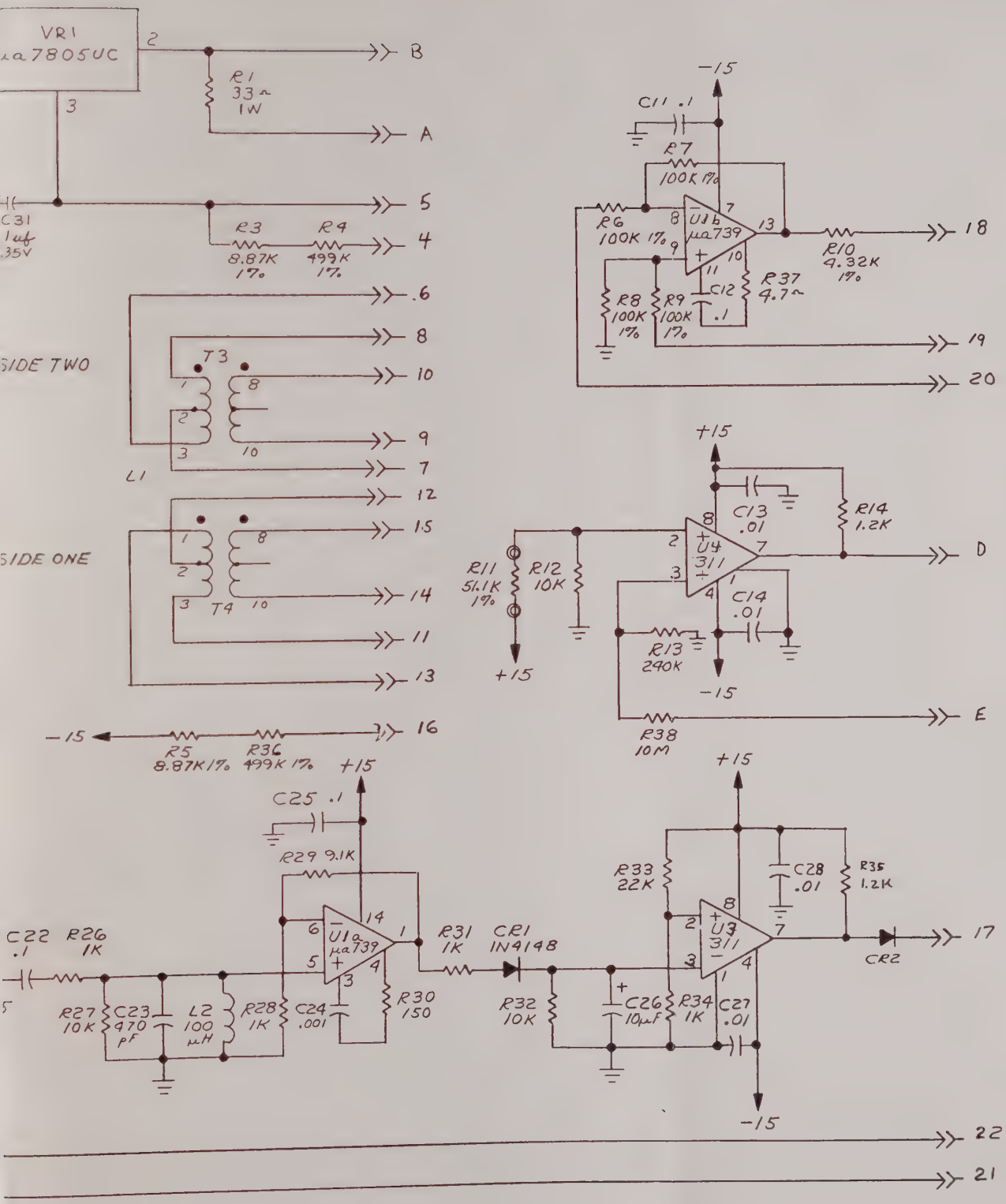

IC1
GB4 ( ) TED
TID REGENERATOR
DUOBINARY LINE DRIVER
DUOBINARY REFERENCE CIRCUIT
IC8
IC7
T1
T4
Y1
4.42pF
+5.5
-6.2
+5.5V
D1+
D1-
D2+
D2-
C2
30, 31
33 -6.2
32 +5.5




T1C/T1D T1D/T1C Converter
Board (A3) Schematic
T1D-106

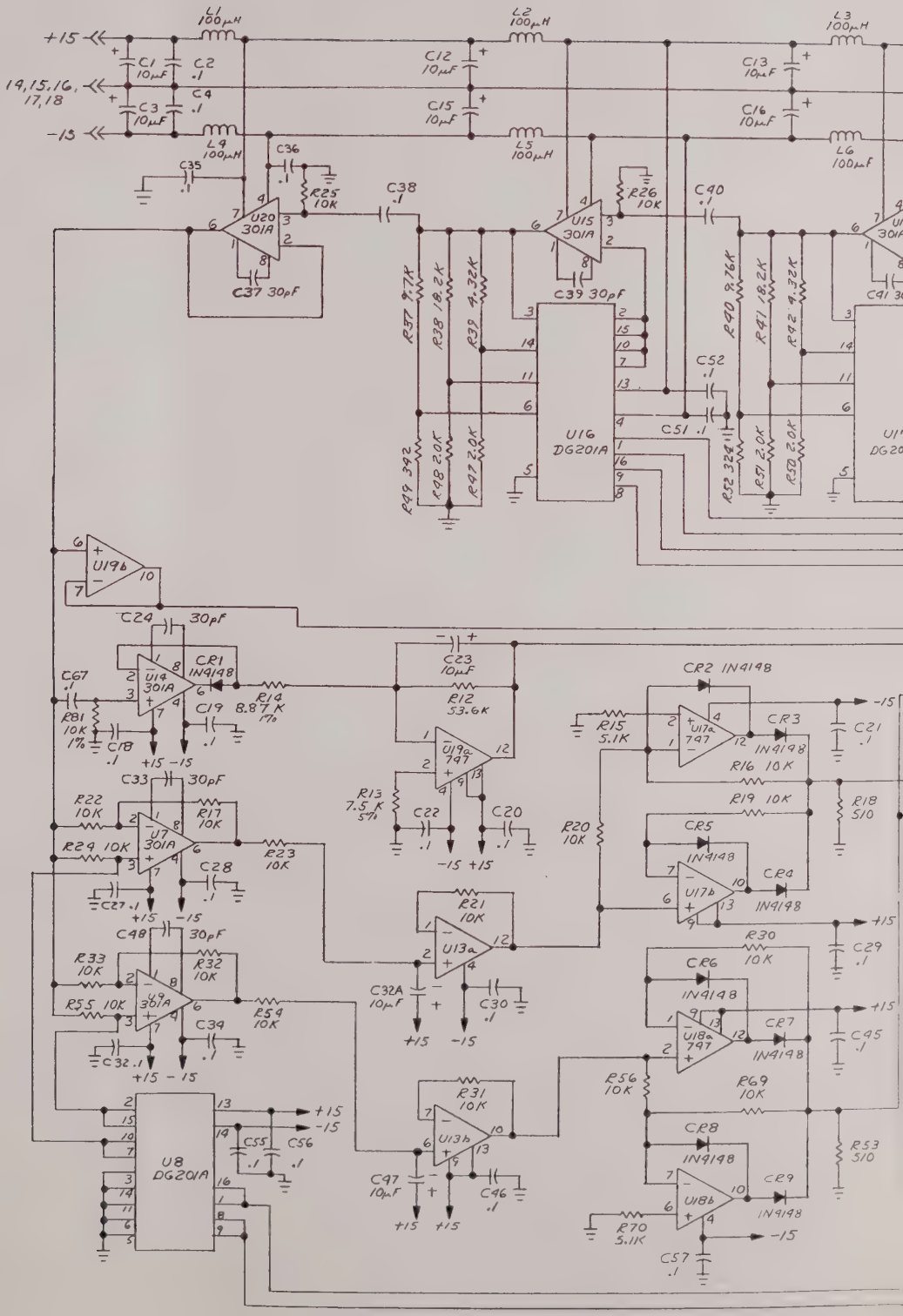
Fig. 5-5

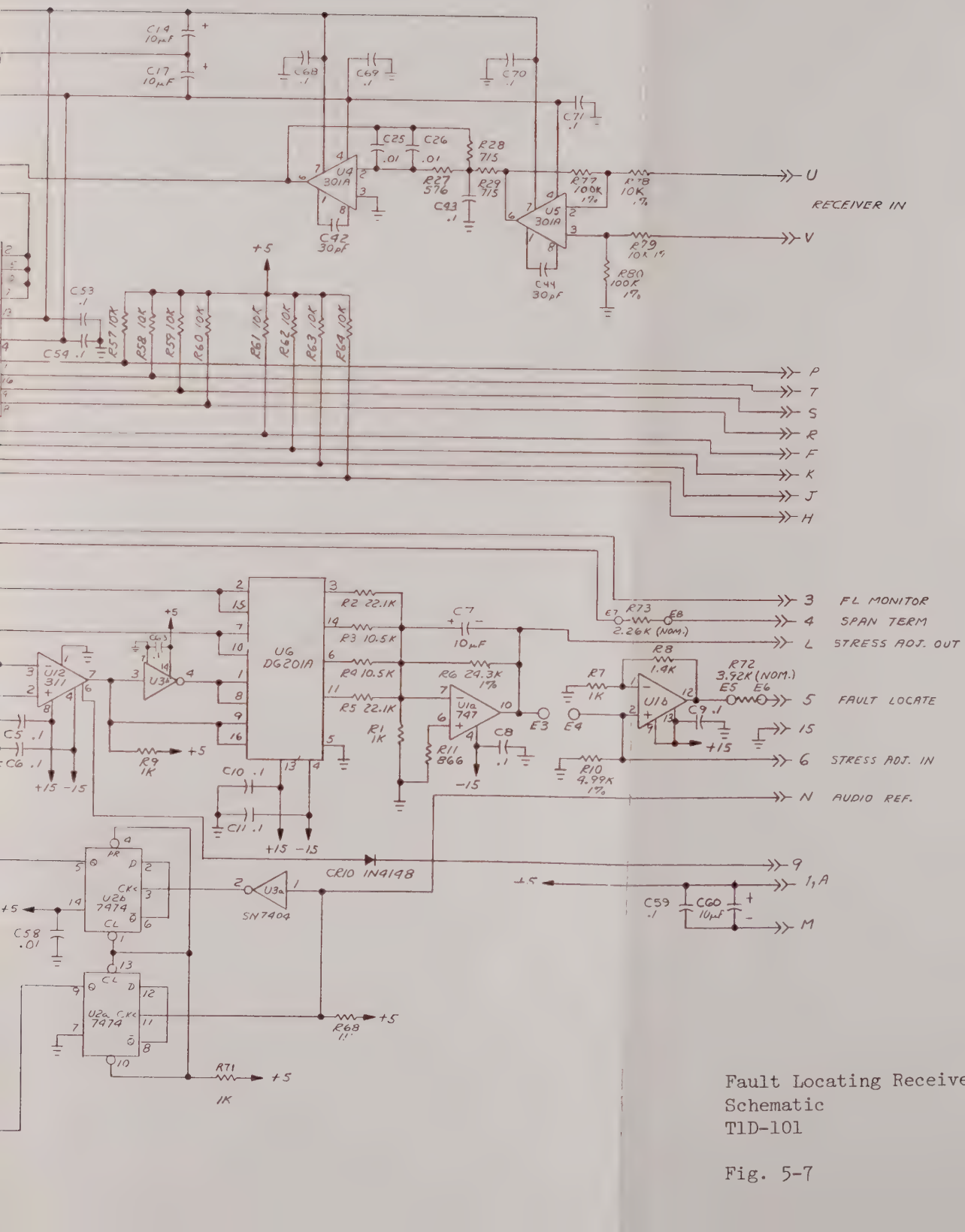

+6.2
T
C1 .01
C2 50μF
C3 .01
C4 50μF
+15
2
-6.2
U
C5 .01
C6 50μF
V
C7 .01
C8 50μF
-15
C
+15
-15
C9 10μF 50V
R
S
T2
P
N
M
T1
J
H
F
K
L
T5
C15 4.7μF
Q1 2N4091
+6.2
C16 390pF
C17 .1
R20 9.09K 1%
C18 .001
R21 150
C19 390pF
C20 .1
R24 9.09K 1%
C21 .001
R15 240
R16 1M
R17 750
R18 1K
R19 1K
R22 1K
R23 1K
-6.2




Repeater Interface Board (A4)
Schematic
T1D-102

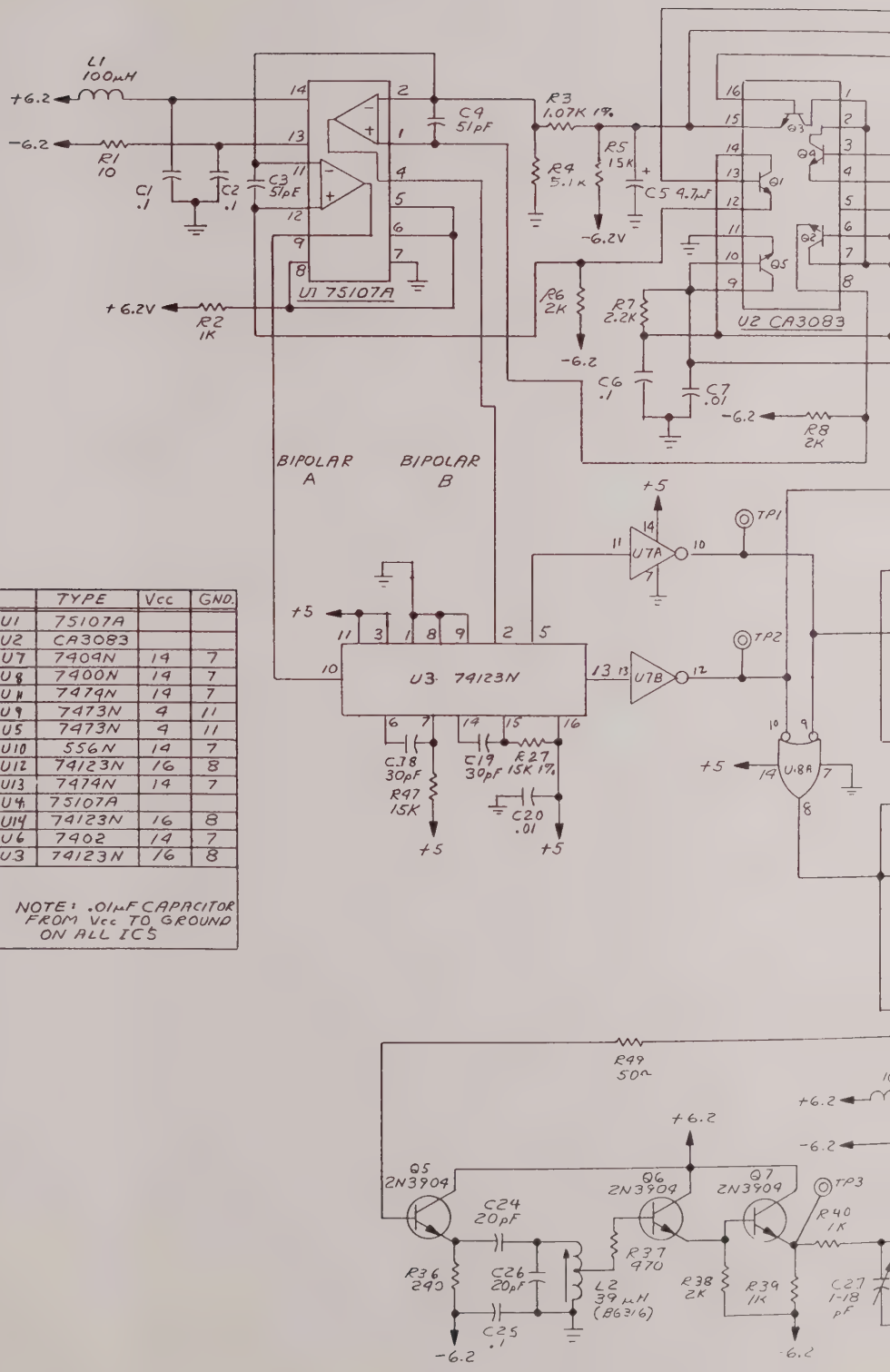
Fig. 5-6


+15
14,15,16,17,18
-15
L1 100μH
L2 100μH
L3 100μH
L4 100μH
L5 100μH
L6 100μH
L9 100μH
C1 10μF
C2 .1
C3 10μF
C4 .1
C12 10μF
C15 10μF
C13 10μF
C16 10μF
C35 .1
C36 .1
C38 .1
C40 .1
C51 .1
C52 .1
R25 10K
R26 10K
U20 301A
U15 301A
C37 30pF
C39 30pF
R37 9.76K
R38 18.2K
R39 9.32K
R40 9.76K
R41 18.2K
R42 9.32K
R49 392
R48 2.0K
R47 2.0K
R51 2.0K
R50 2.0K
R52 324
U16 DG201A
C24 30pF
C67 .1
R81 10K 1%
C18 .1
U14 301A
CR1 IN4148
R14 8.87K 1%
C19 .1
C23 10μF
R12 53.6K
U19a 747
R13 7.5K 5%
C22 .1
C20 .1
CR2 IN4148
R15 5.1K
U17a 747
CR3 IN4198
C21 .1
R16 10K
R19 10K
R18 5.1Ω
R20 10K
CR5 IN4148
U17b
CR4 IN4198
C33 30pF
R22 10K
R17 10K
R24 10K
U7 301A
R23 10K
C28 .1
C27 .1
R21 10K
U13a
C32A 10μF
C30 .1
R30 10K
C29 .1
CR6 IN4148
U18a 747
CR7 IN4198
C45 .1
C48 30pF
R33 10K
R32 10K
R55 10K
U9 301A
R54 10K
C34 .1
C32 .1
R56 10K
R69 10K
CR8 IN4198
CR9 IN4198
R53 5.1Ω
R31 10K
U13b
C55 .1
C56 .1
C47 10μF
C46 .1
U8 DG201A
R70 5.11K
C57 .1
U19b 747
U18b
U17b



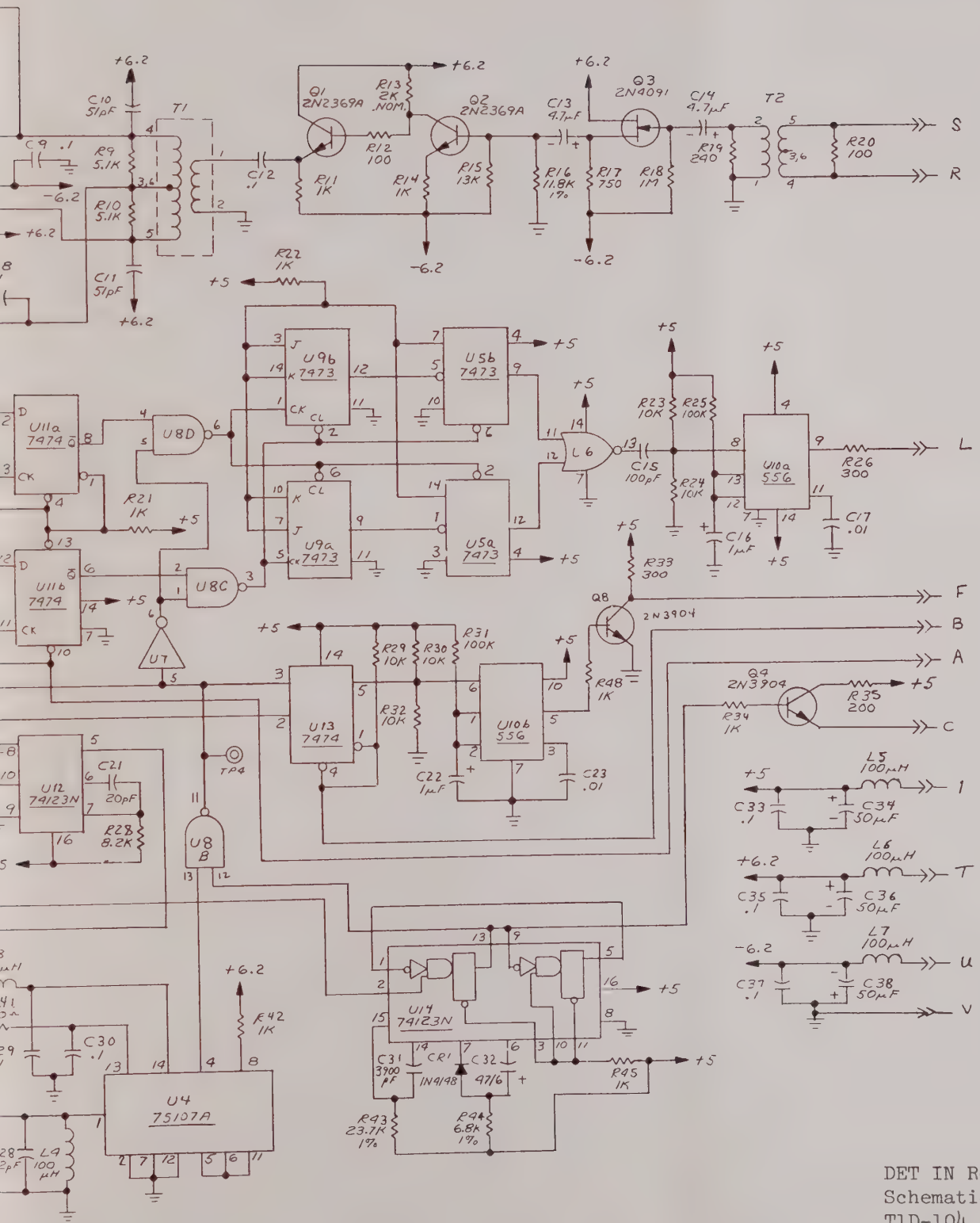

Fault Locating Receiver (A5)
Schematic
T1D-101

Fig. 5-7



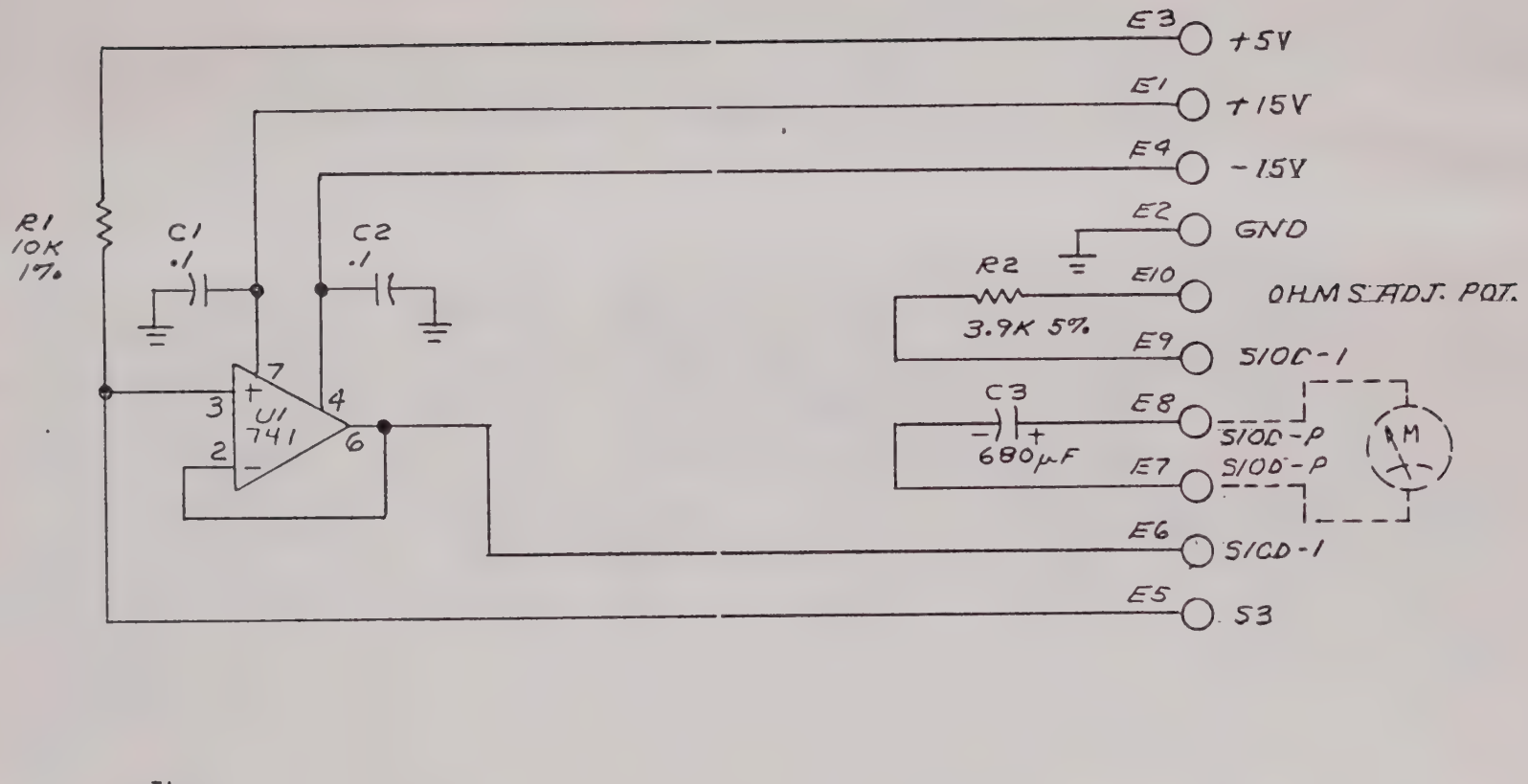

| | TYPE | Vcc | GND. |
|---|---|---|---|
| U1 | 75107A | | |
| U2 | CA3083 | | |
| U7 | 7409N | 14 | 7 |
| U8 | 7400N | 14 | 7 |
| U11 | 7479N | 14 | 7 |
| U9 | 7473N | 4 | 11 |
| U5 | 7473N | 4 | 11 |
| U10 | 556N | 14 | 7 |
| U12 | 74123N | 16 | 8 |
| U13 | 7474N | 14 | 7 |
| U4 | 75107A | | |
| U14 | 74123N | 16 | 8 |
| U6 | 7402 | 14 | 7 |
| U3 | 74123N | 16 | 8 |

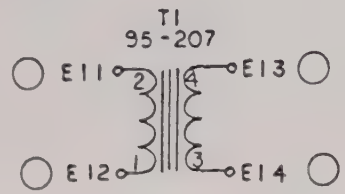
NOTE: .01μF CAPACITOR FROM Vcc TO GROUND ON ALL ICS




DET IN Receiver (A6)
Schematic
T1D-104

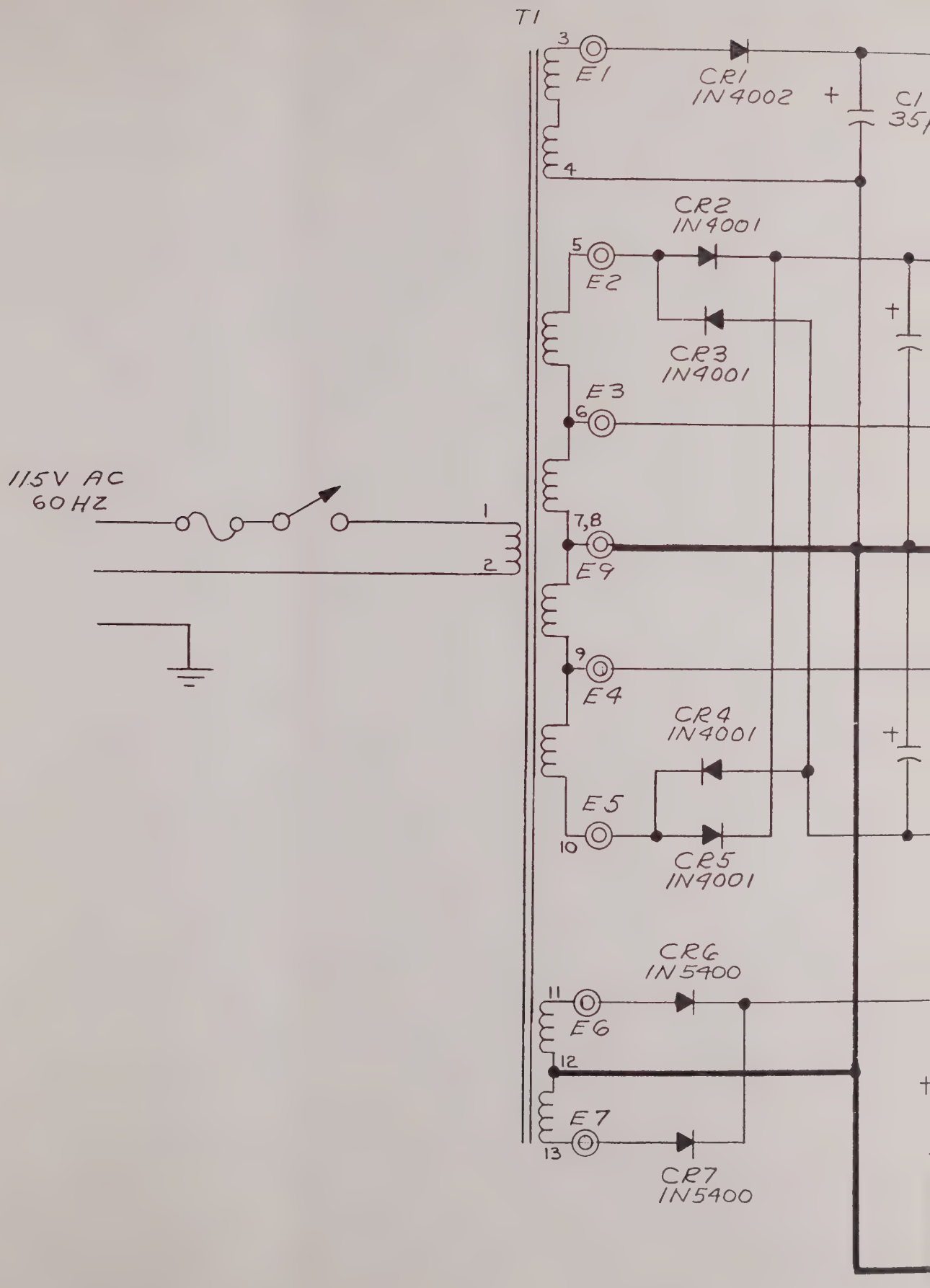
Fig. 5-8

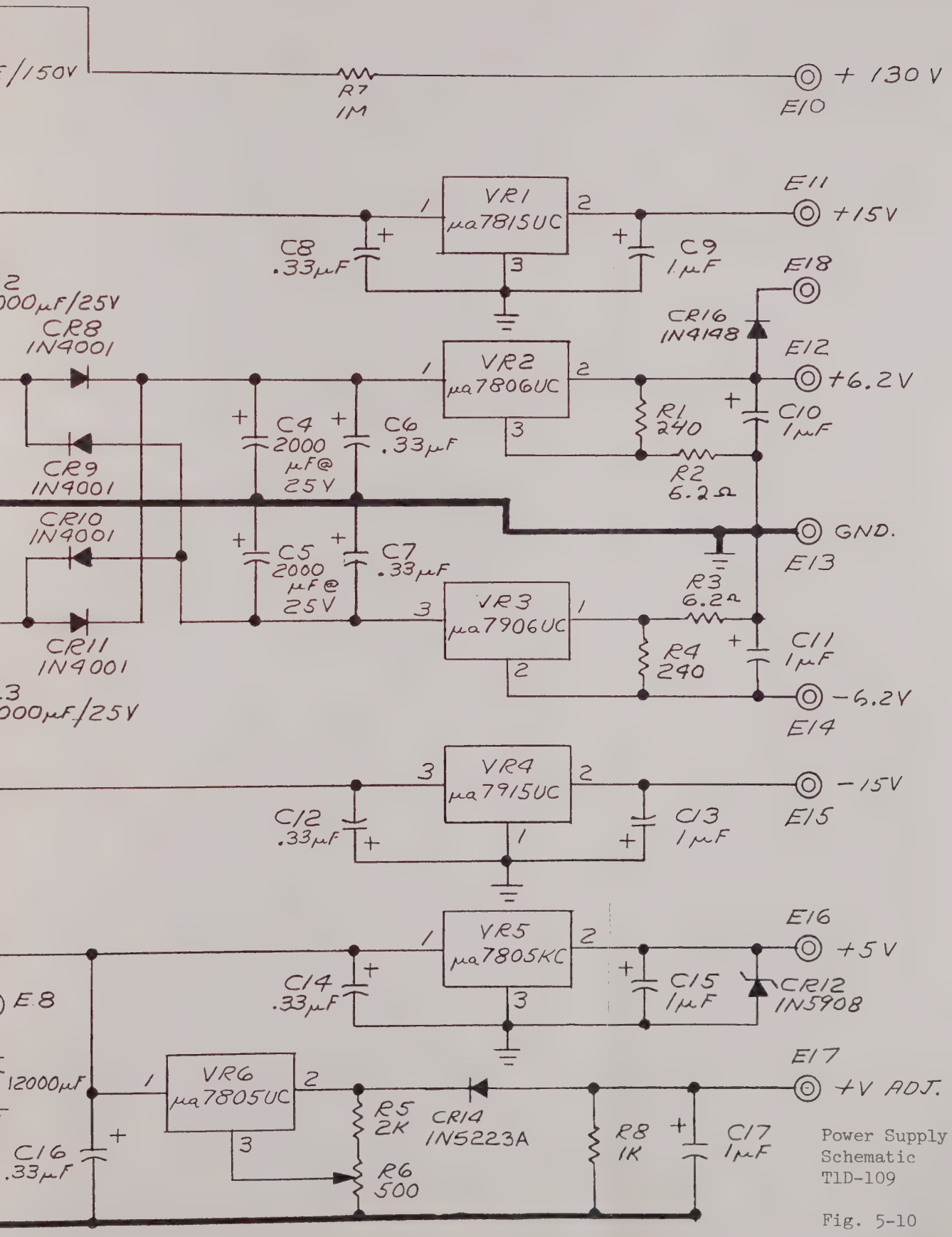



Meter Interface Board (A7)
Schematic
T1D-107

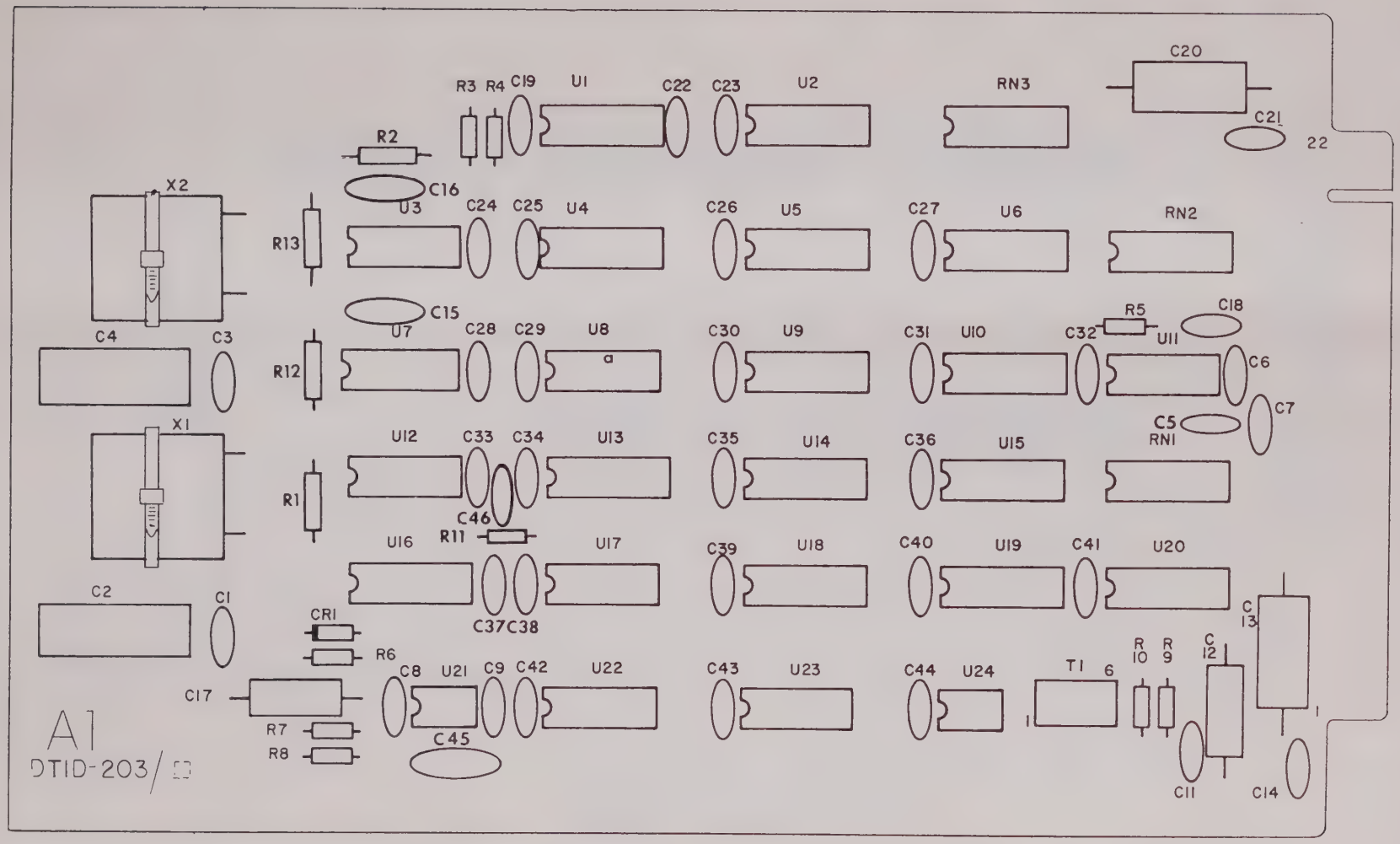
Fig. 5-9


T1
3
E1
CR1
IN4002
+
C1
35
4
CR2
IN4001
5
E2
CR3
IN4001
E3
6
115V AC
60HZ
1
2
7,8
E9
9
E4
CR4
IN4001
E5
10
CR5
IN4001
CR6
IN5400
11
E6
12
E7
13
CR7
IN5400



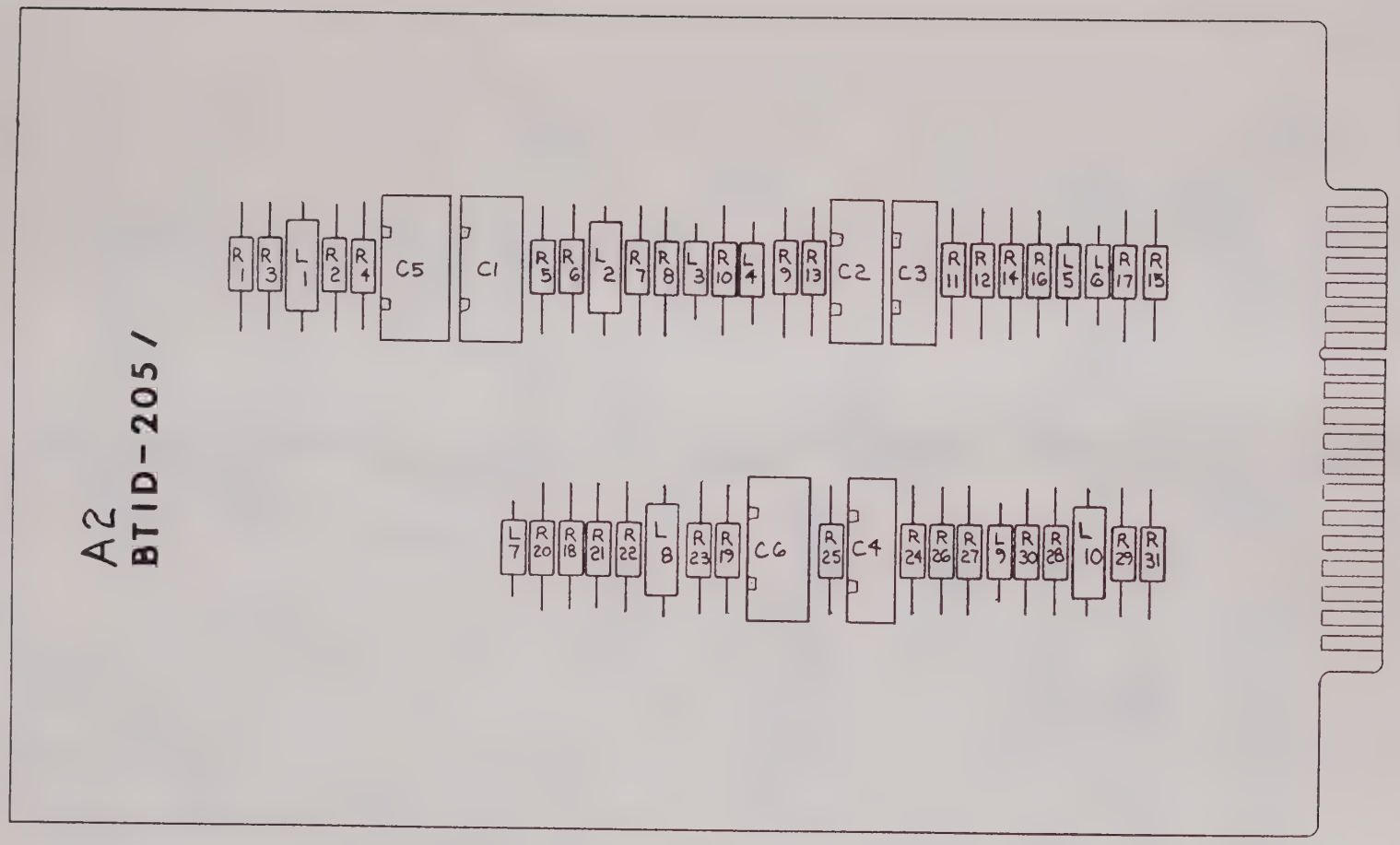

Power Supply (A8)
Schematic
T1D-109

Fig. 5-10



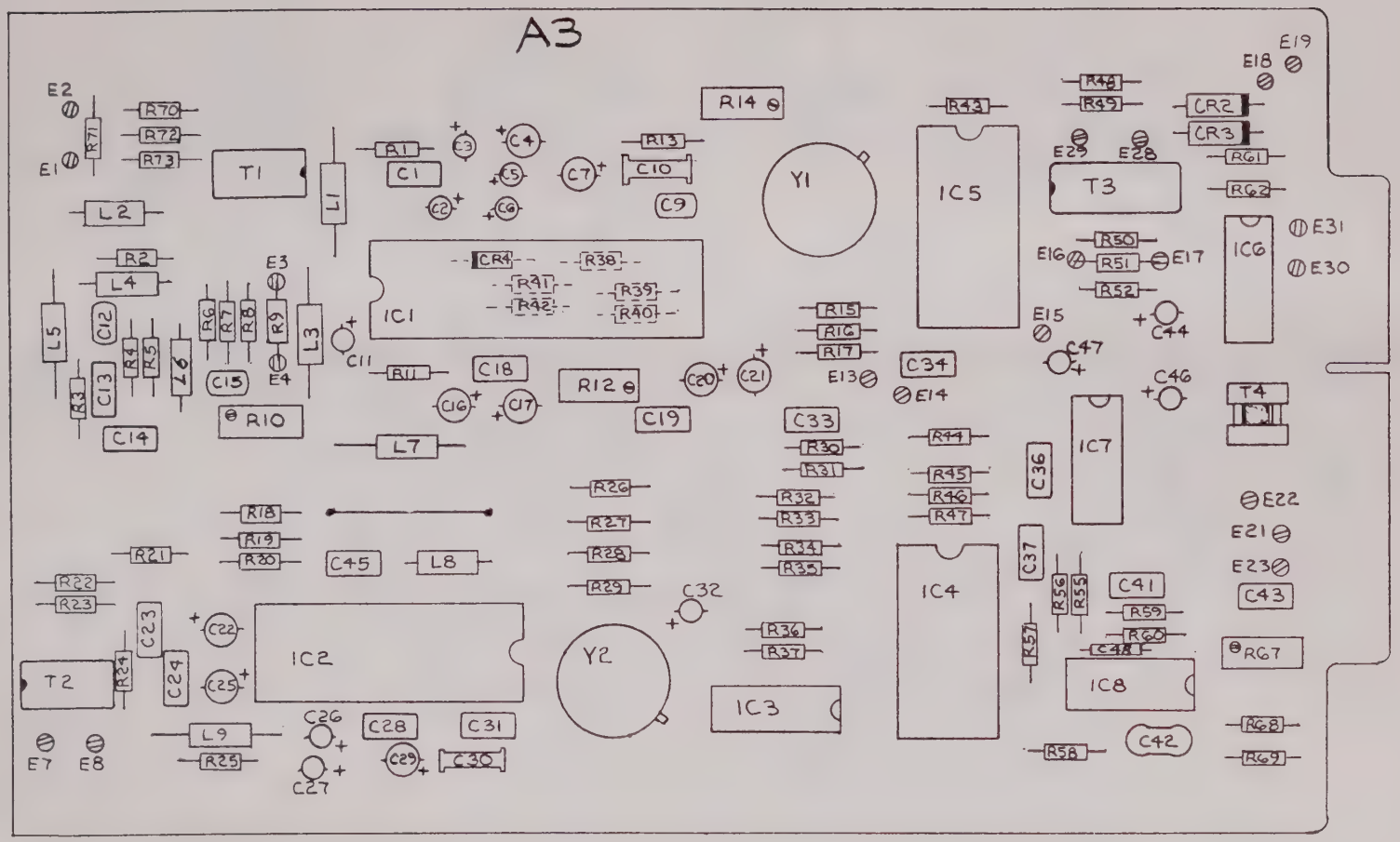

Transmitter Board (A1)
Assembly Drawing
T1D-203

Fig. 5-11



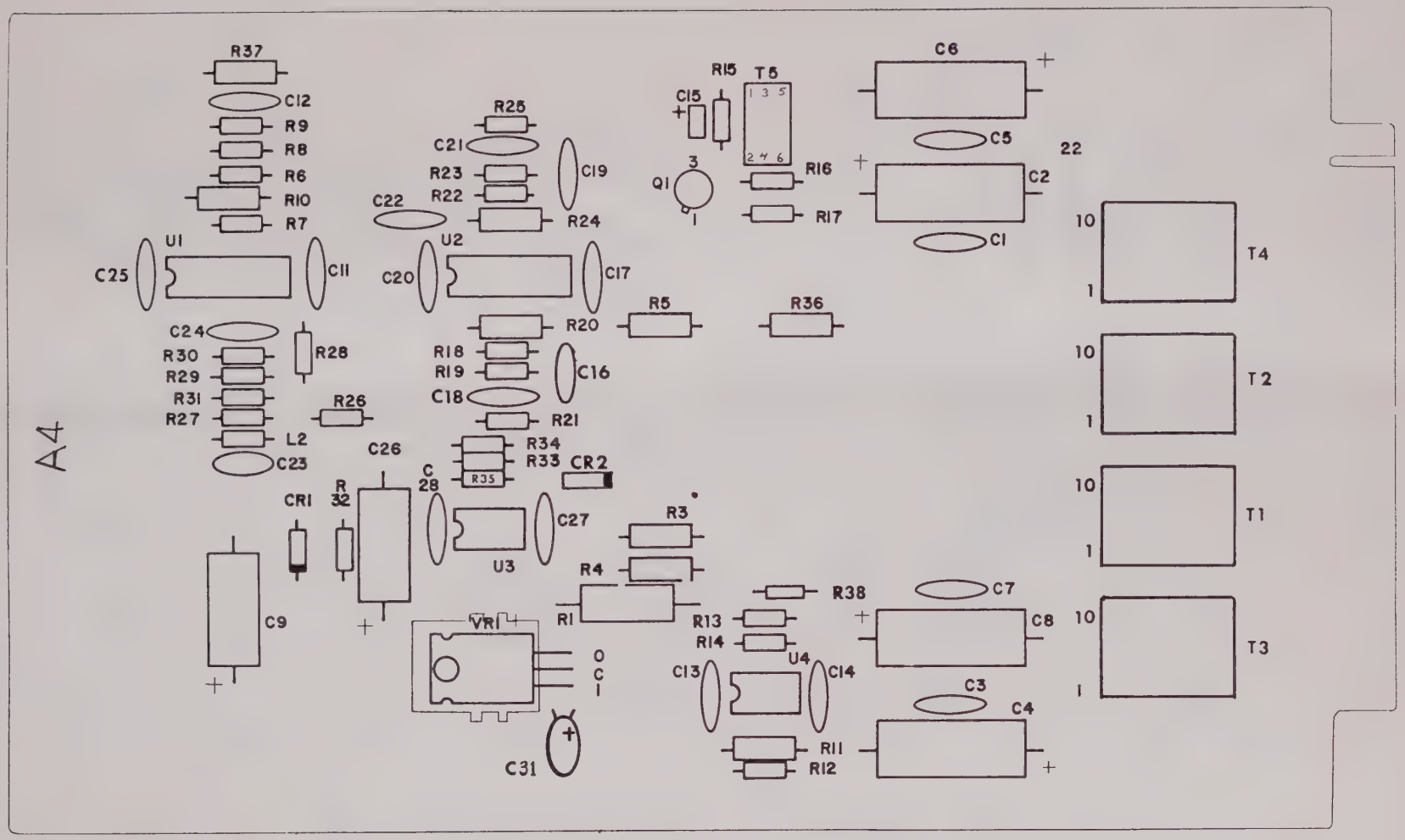

Artificial Line Board (A2)
Assembly Drawing
T1D-205

Fig. 5-12



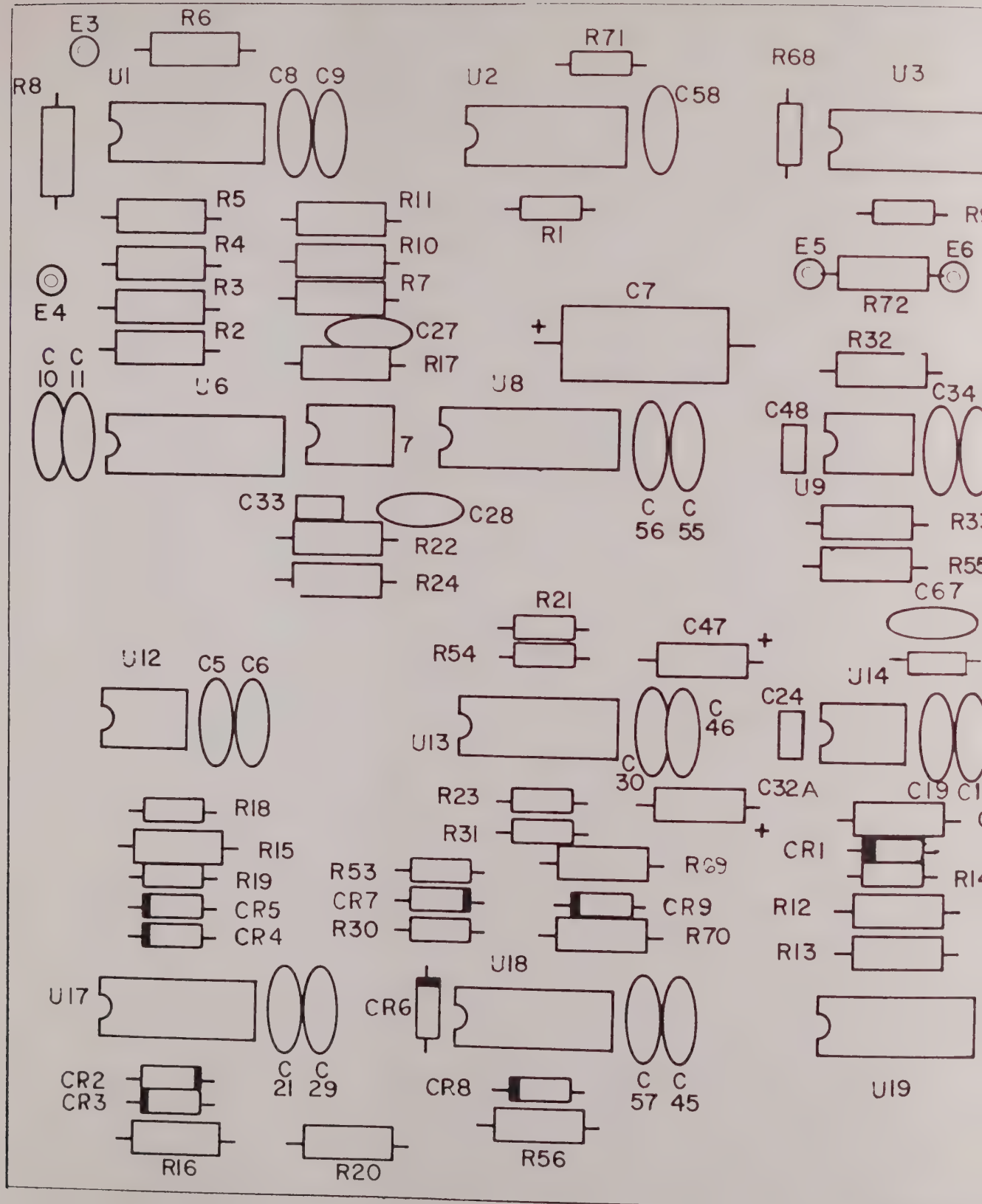

T1C/T1D T1D/T1C Converter
Board (A3) Assembly Drawing
T1D-206

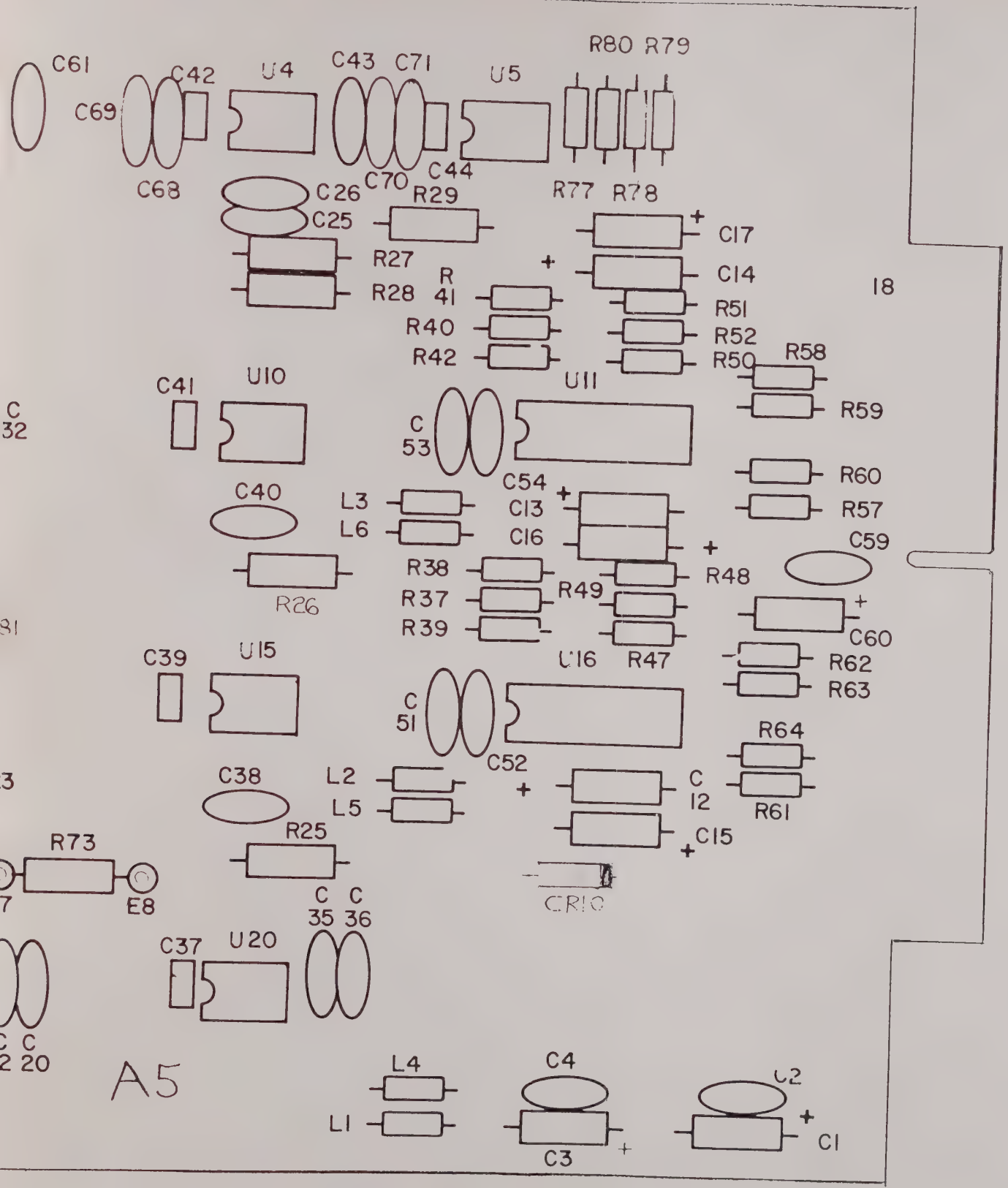
Fig. 5-13




Repeater Interface Board (A4)
Assembly Drawing
T1D-202

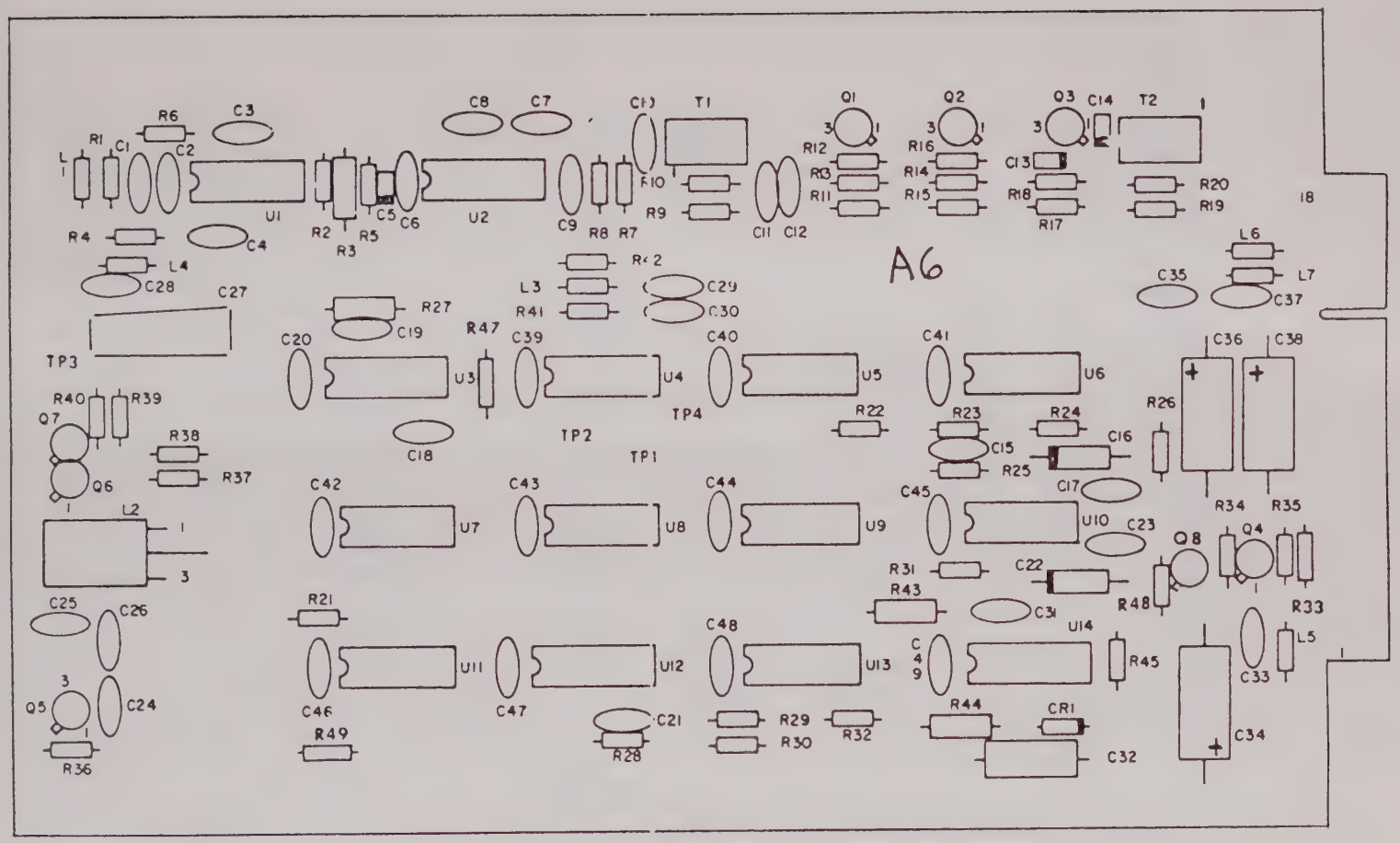
Fig. 5-14


E3
R6
R8
U1
C8 C9
R71
U2
C58
R68
U3
R5
R4
R3
R2
R11
R10
R7
C27
R17
R1
E4
E5
E6
R72
C7
R32
C34
C 10
C 11
U6
7
U8
C48
U9
C33
C28
R22
R24
C 56
C 55
R21
R54
C47
C67
U12
C5 C6
U14
C24
U13
C 46
C 30
C32A
C19
R23
R31
R69
R18
R15
R19
CR5
CR4
R53
CR7
R30
CR9
R70
CR1
R12
R13
U17
U18
CR6
C 21
C 29
C 57
C 45
CR2
CR3
CR8
R16
R20
R56
U19



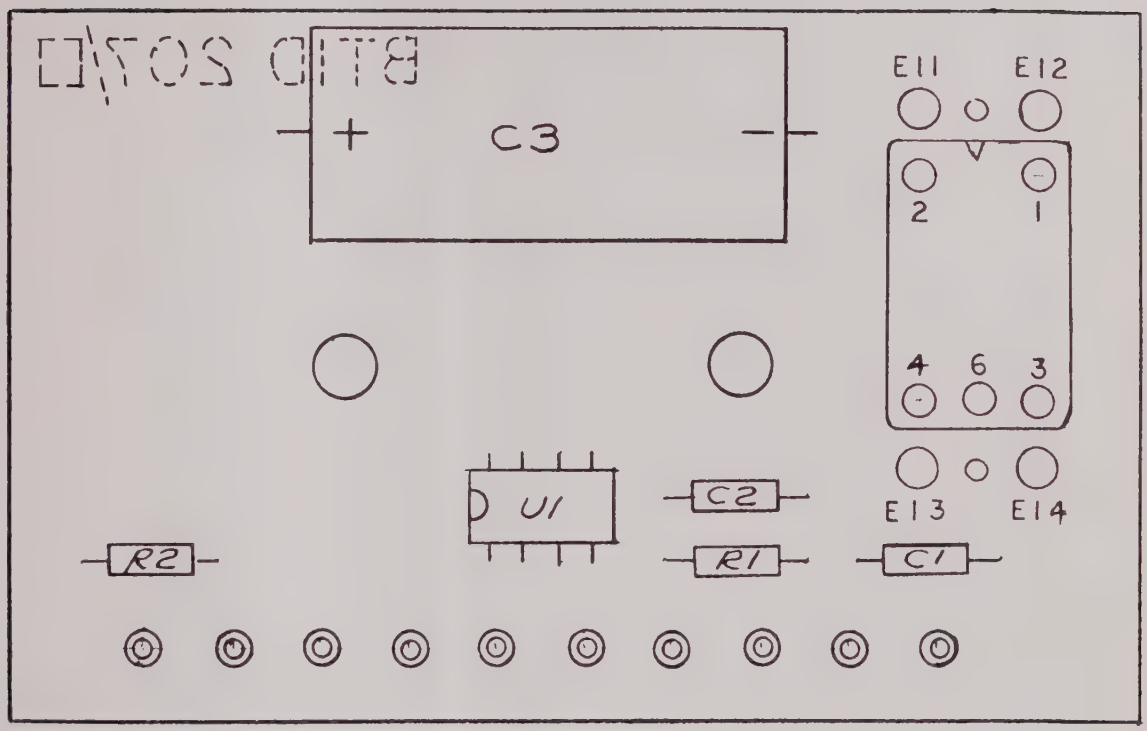

Fault Locating Receiver (A5)
Assembly Drawing
T1D-201

Fig. 5-15




DET IN Receiver (A6)
Assembly Drawing
T111-204

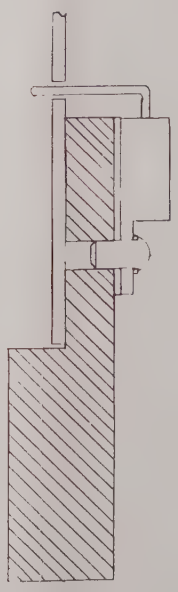
Fig. 5-16




Meter Interface Board (A7)
Assembly Drawing
T1D-207

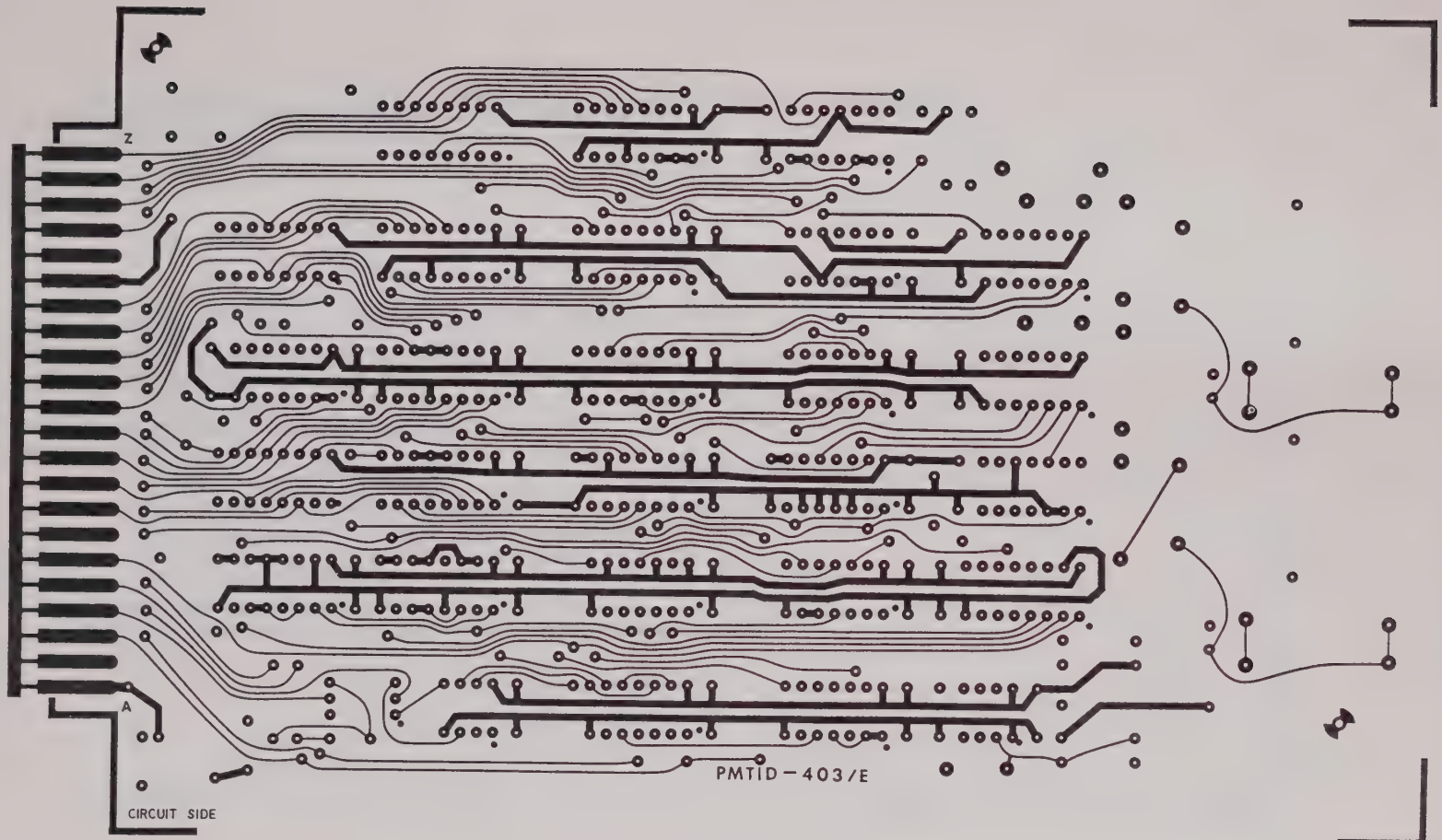
Fig. 5-17

E9
E8
E7
E6
E5
E4
E3
E2
E1
E17
E16
CR7
CR6
CR5
CR4
CR11
CR10
CR8
CR9
CR2
CR3
CR1
C3
C5
C4
C16
C14
C15
C13
C12
C11
C7
R3
R5
R6
CR14
R8
C17
CR12
A
VR6
VR4
VR3
VR5



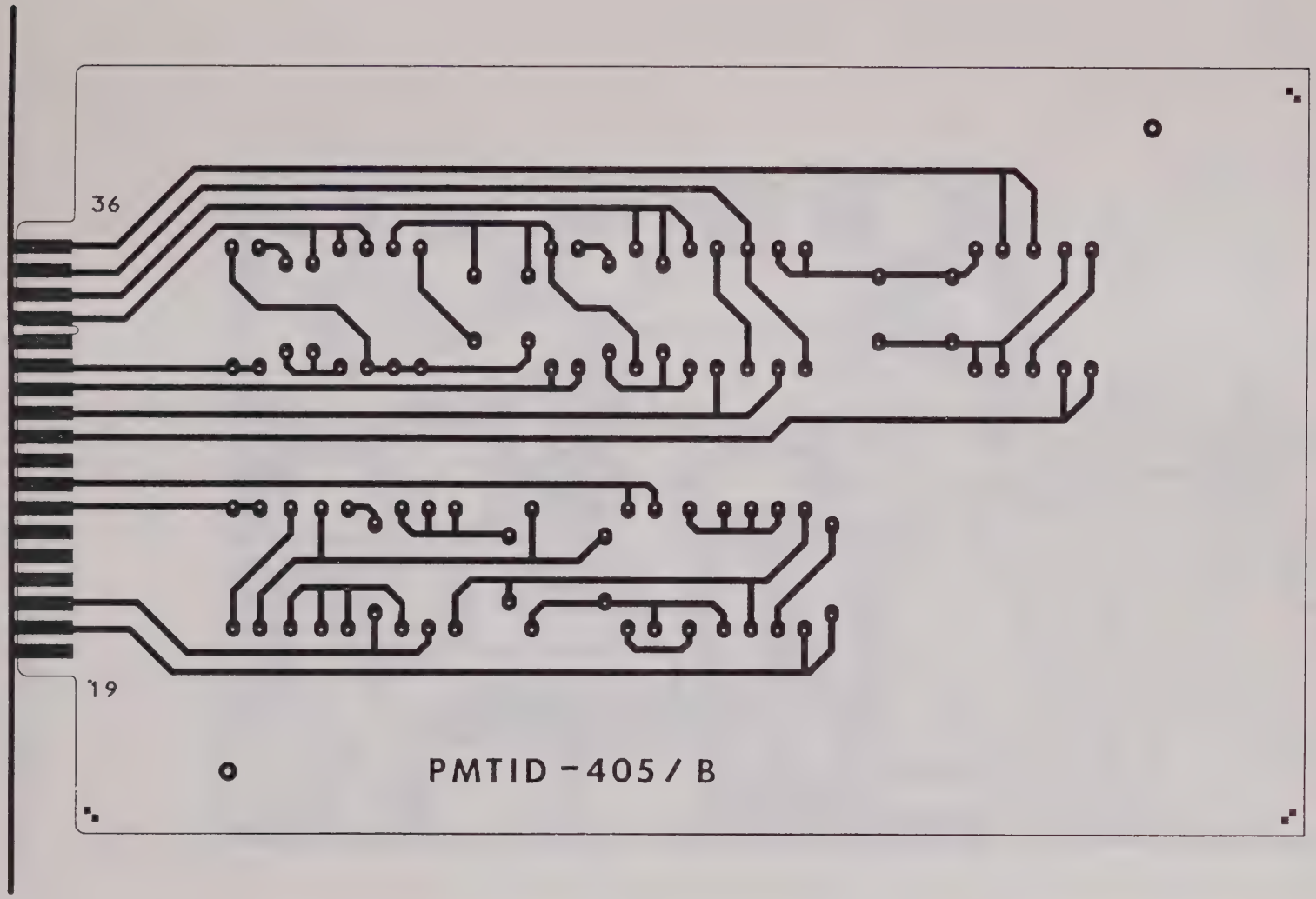
Power Supply Board (A8)
Assembly Drawing
T1D-209

Fig. 5-18




Transmitter Board (A1)
Circuit Pattern
(Non-Component Side)
PMT1D-403

Fig. 5-20

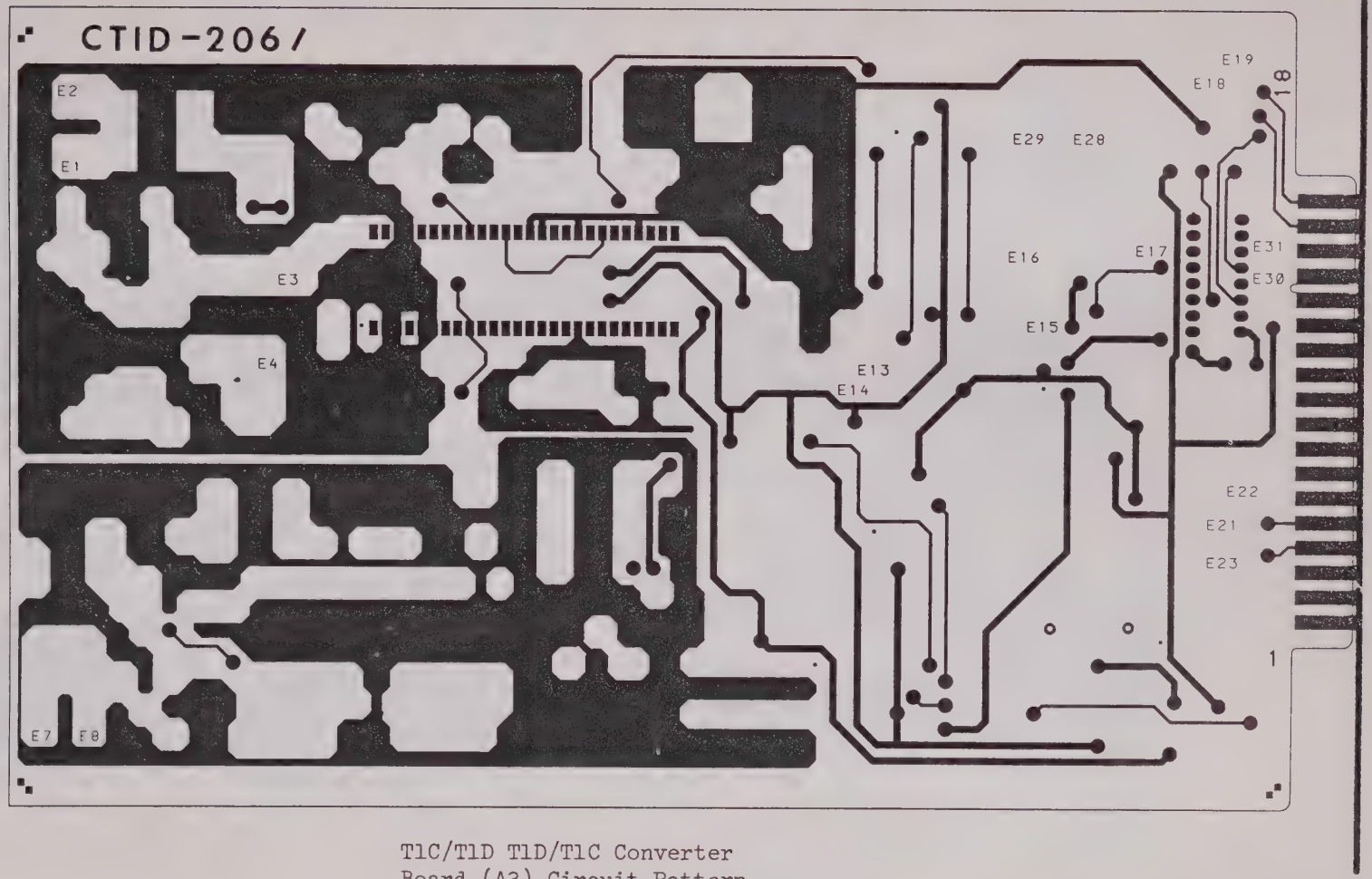



NONCOMPONENT SIDE

Artificial Line Board (A2)
Circuit Pattern
(Non-Component Side)
PMT1D-405

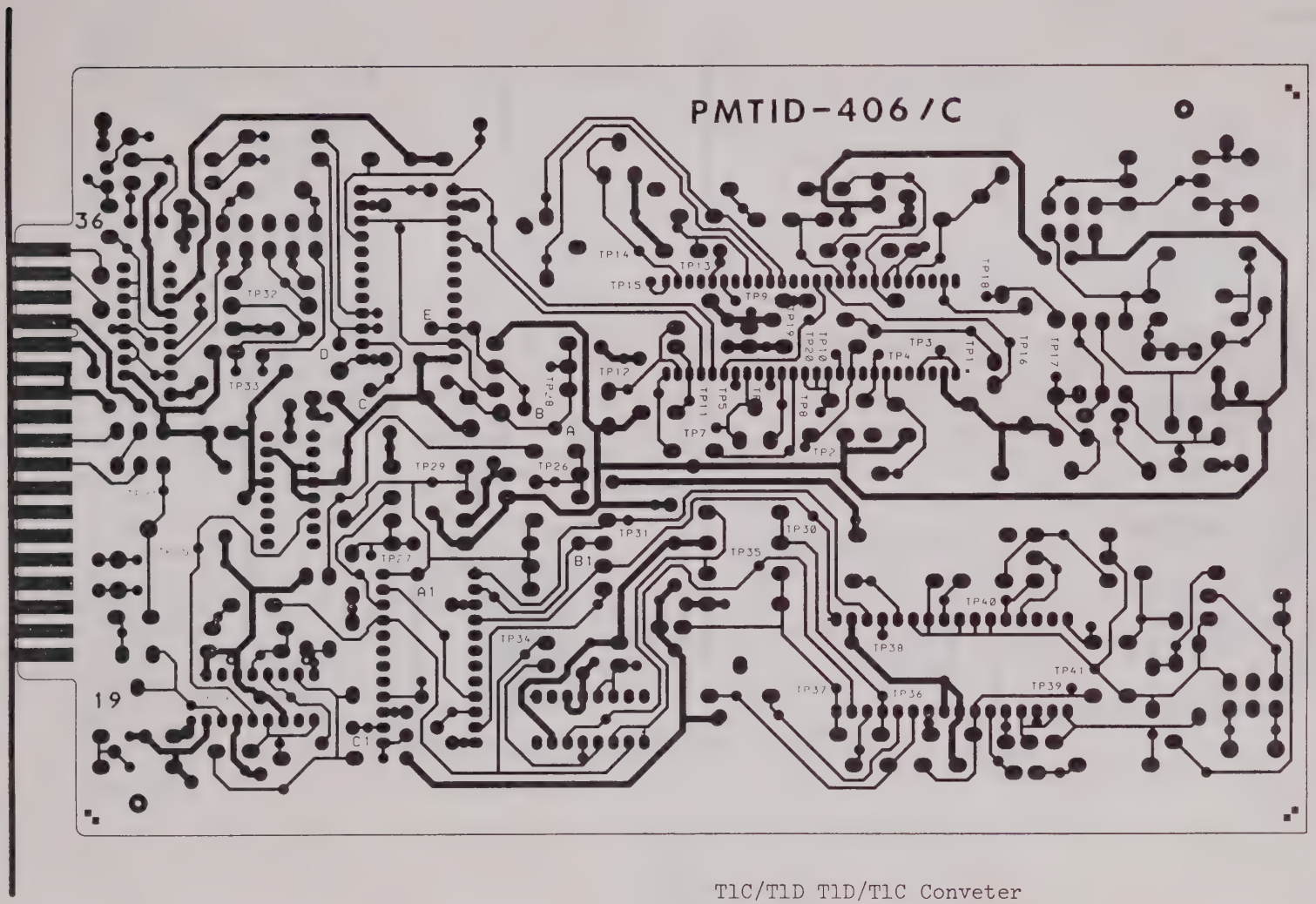
Fig. 5-21

COMPONENT SIDE




T1C/T1D T1D/T1C Converter
Board (A3) Circuit Pattern
(Component Side)
PMT1D-406

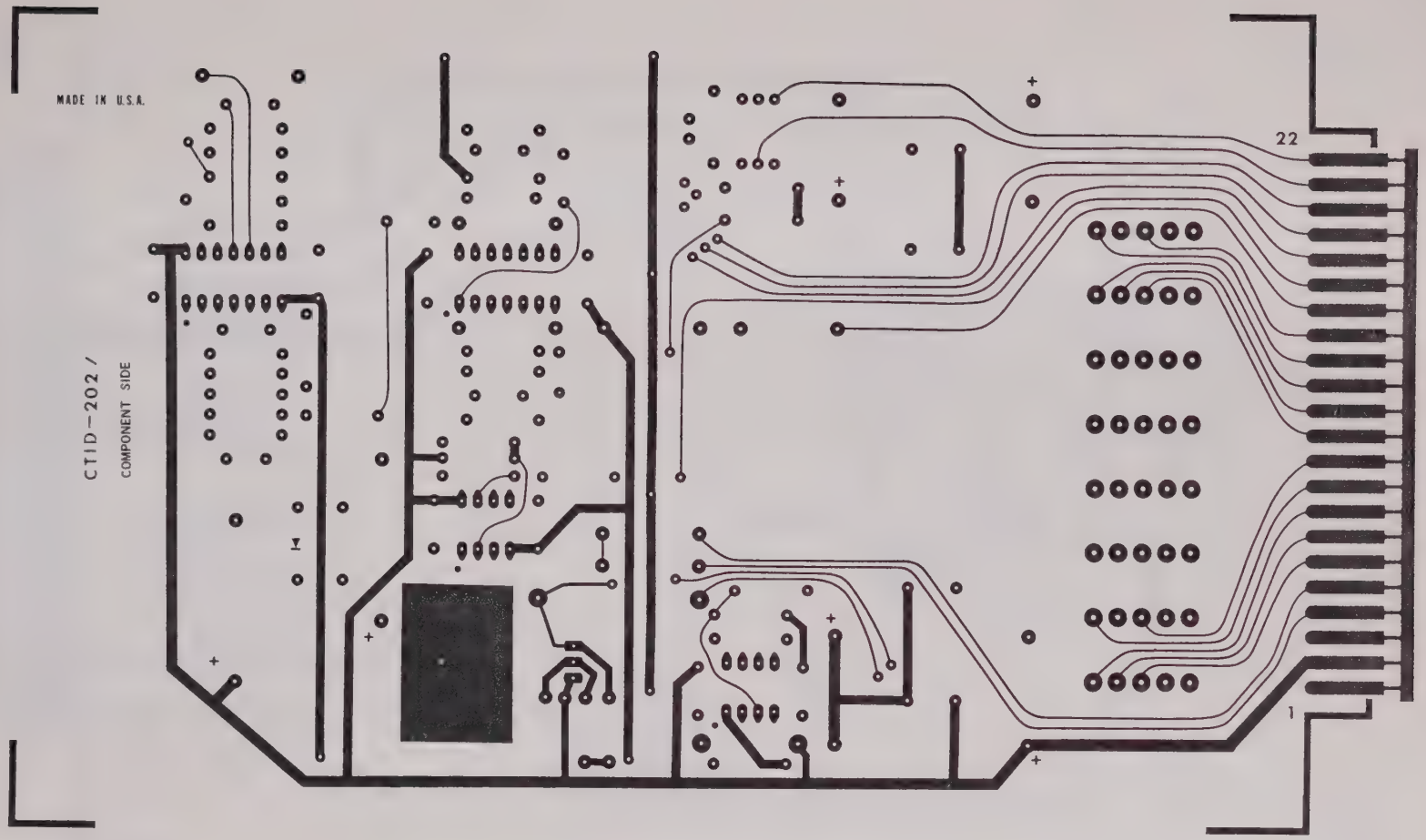
Fig. 5-22




T1C/T1D T1D/T1C Conveter
Board (A3) Circuit Pattern
(Non-Component Side)
PMT1D-406

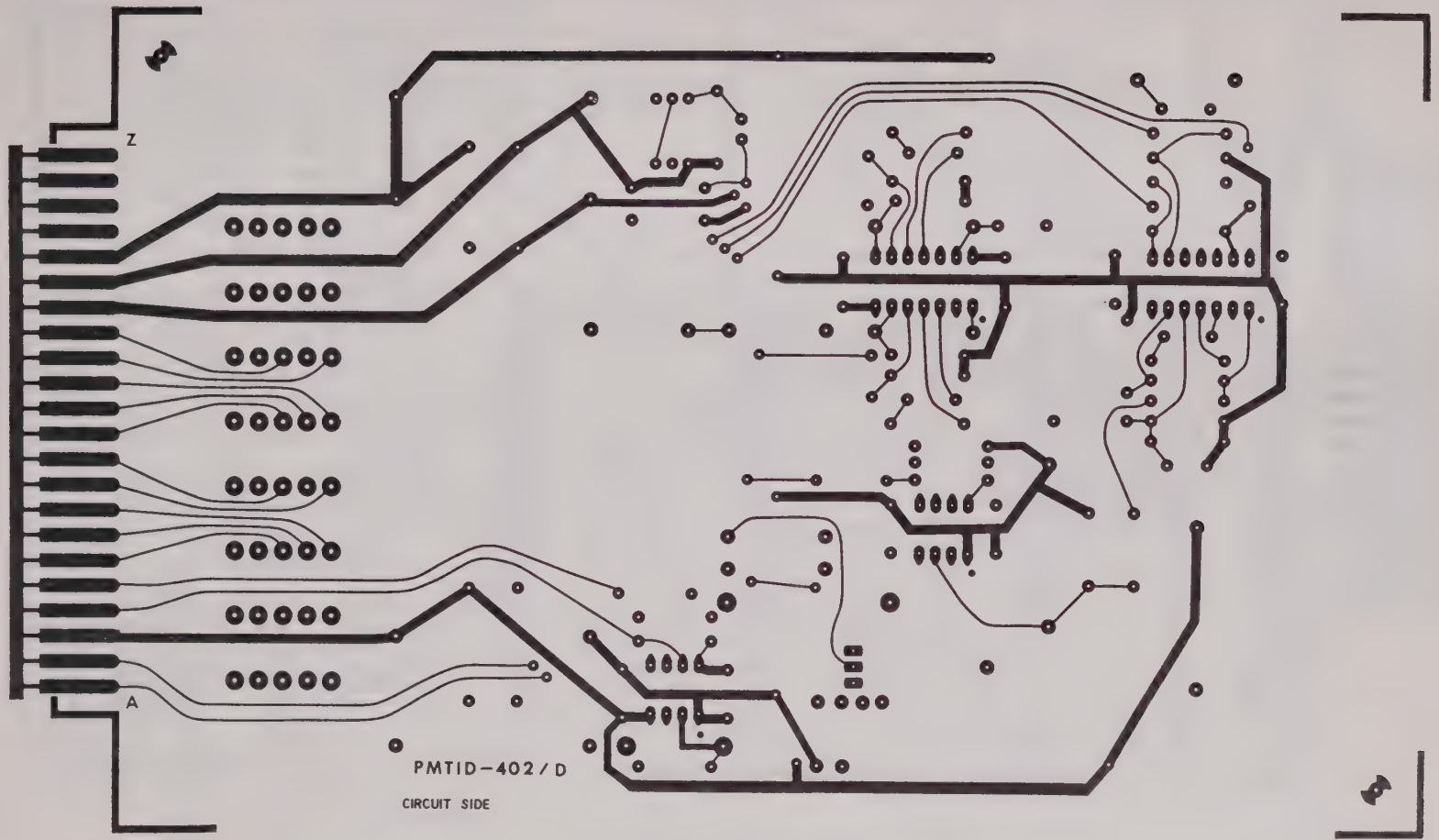
Fig. 5-23

NONCOMPONENT SIDE



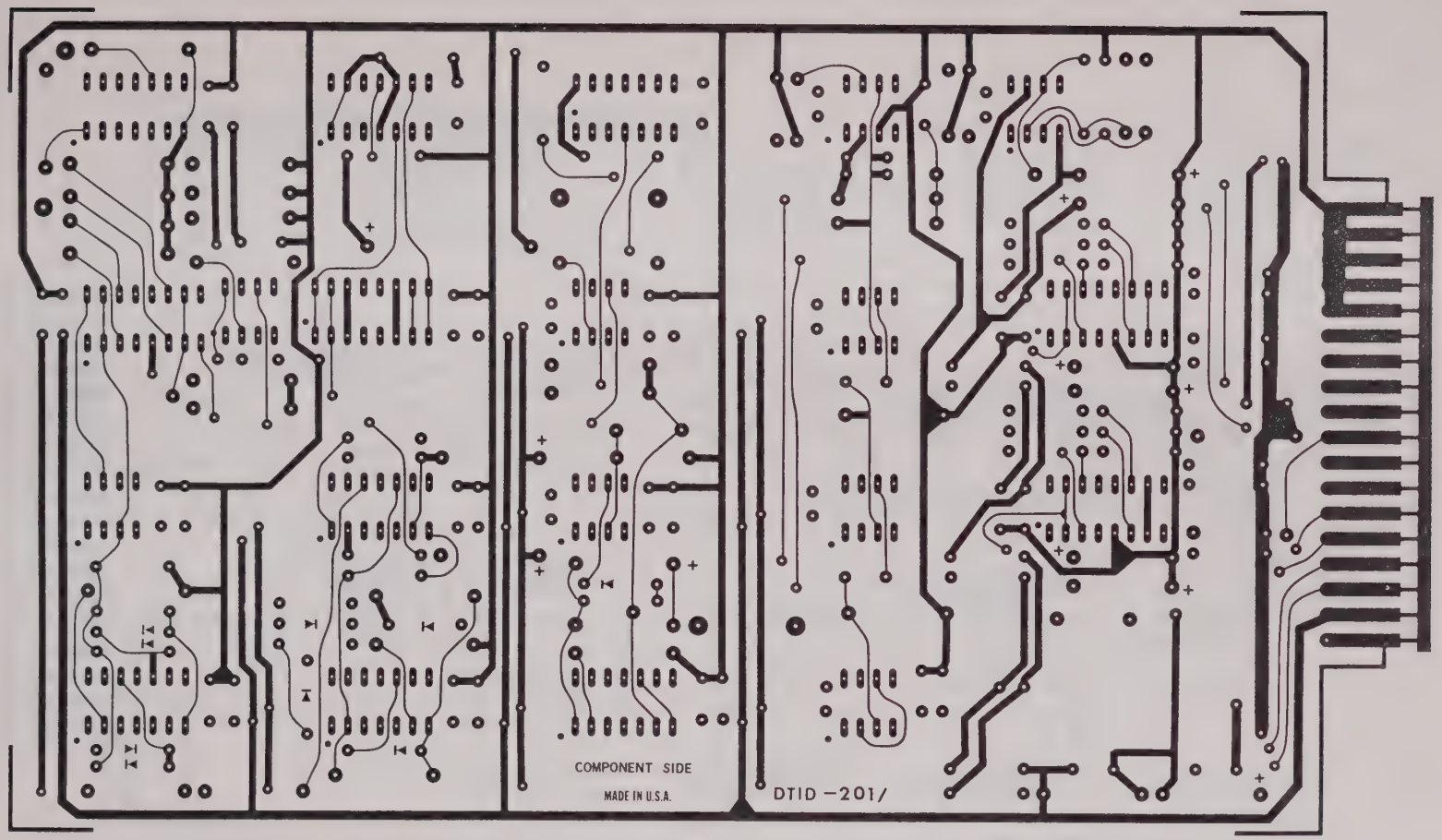

Repeater Interface Board (A4)
Circuit Pattern
(Component Side)
PMT1D-402

Fig. 5-24



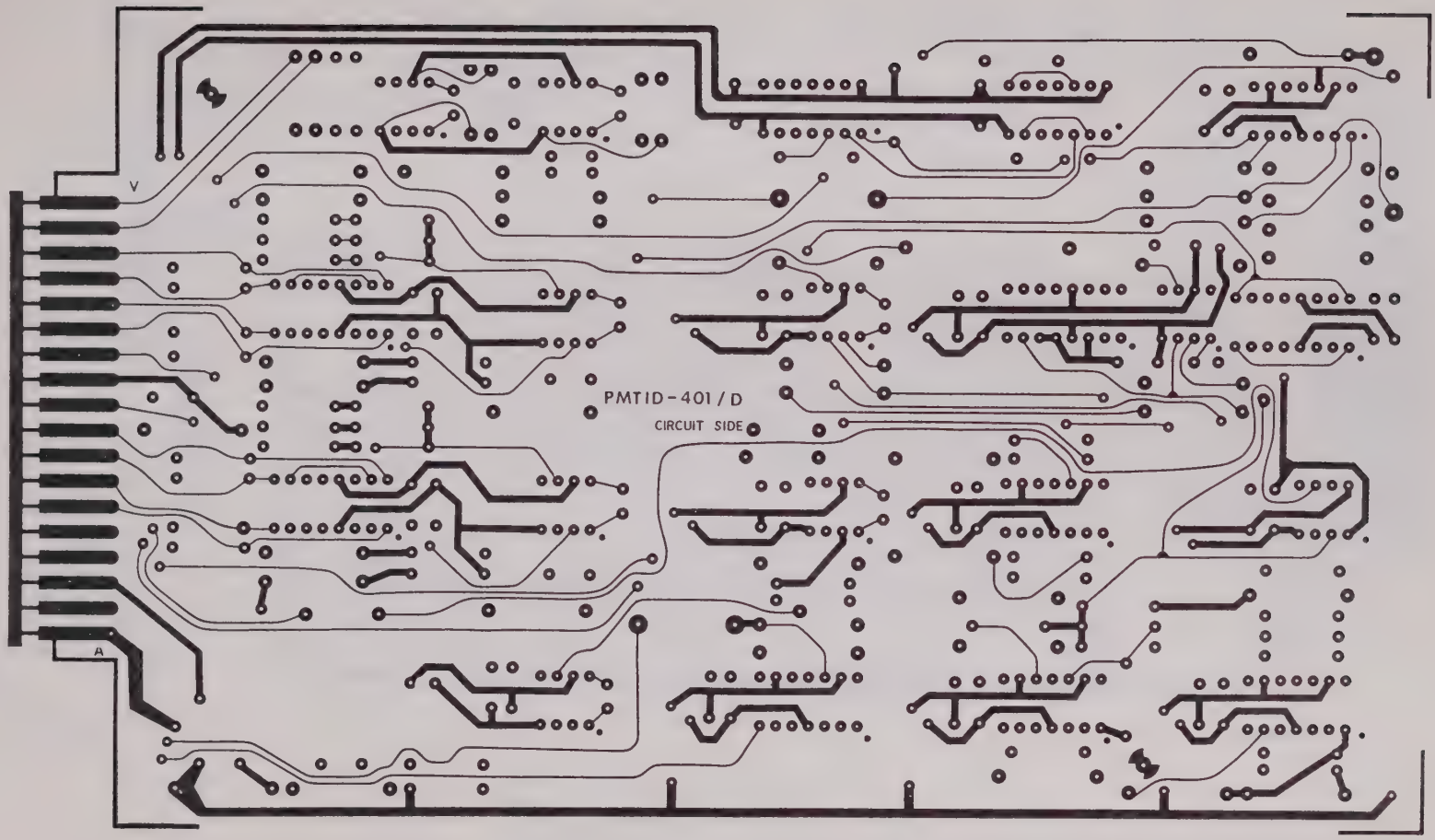

Repeater Interface Board (A4)
Circuit Pattern
(Non-Component Side)
PMT1D-402

Fig. 5-25



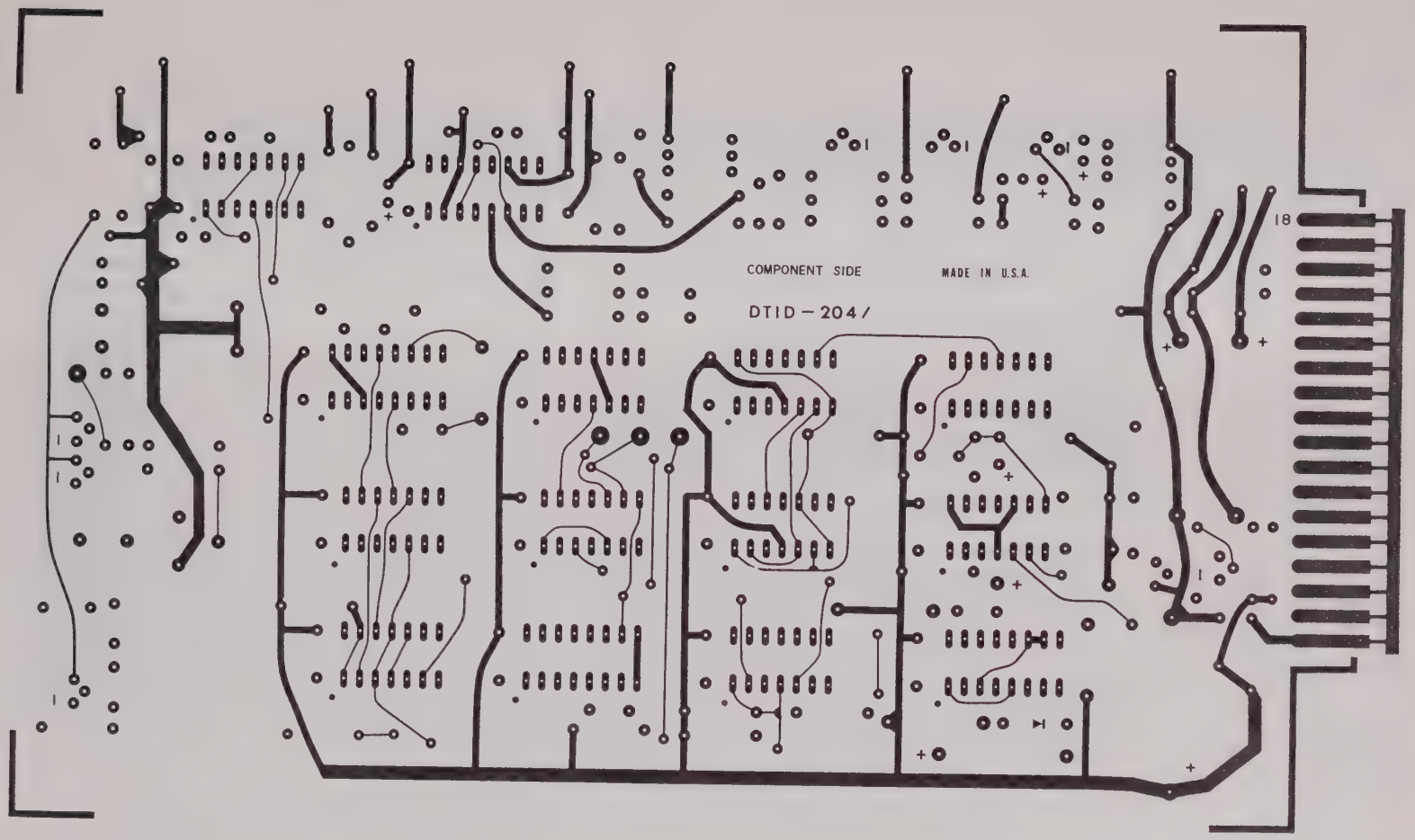

Fault Locating Receiver Board (A5)
Circuit Pattern
(Component Side)
PMT1D-401

Fig. 5-26



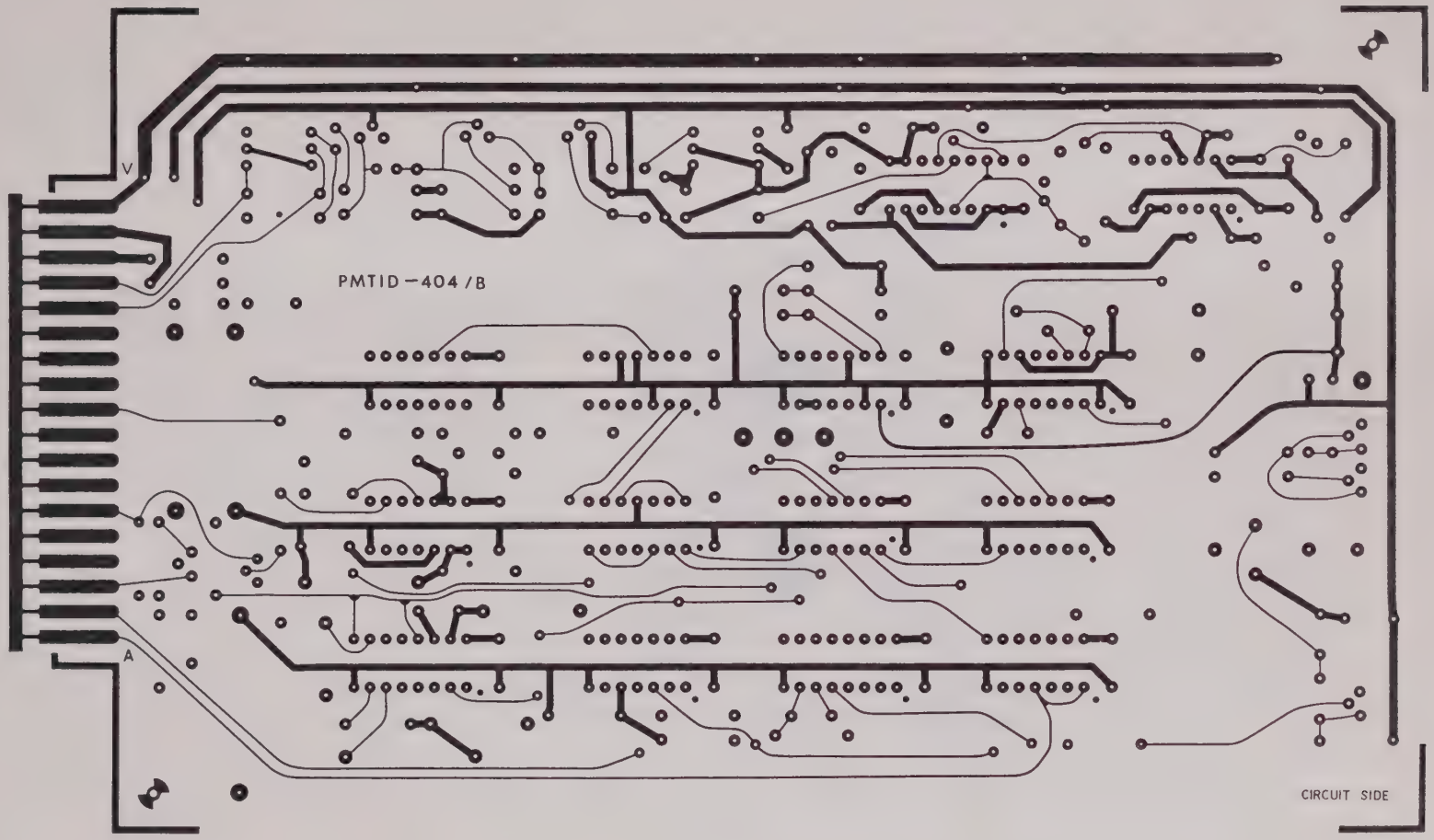

Fault Locating Receiver Board (A5)
Circuit Pattern
(Non-Component Side)
PMTID-401

Fig. 5-27



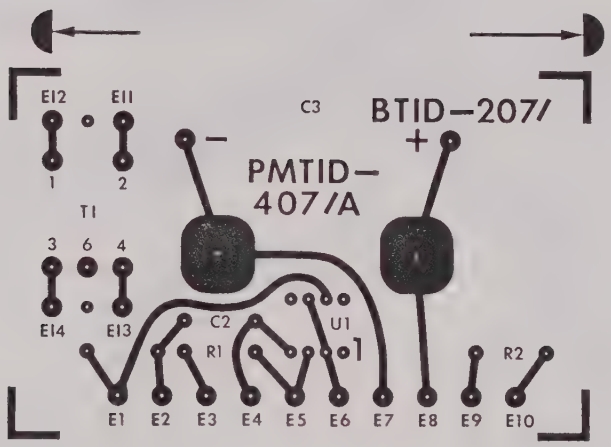

DET IN Receiver Board (A6)
Circuit Pattern
(Component Side)
PMT1D-404

Fig. 5-28



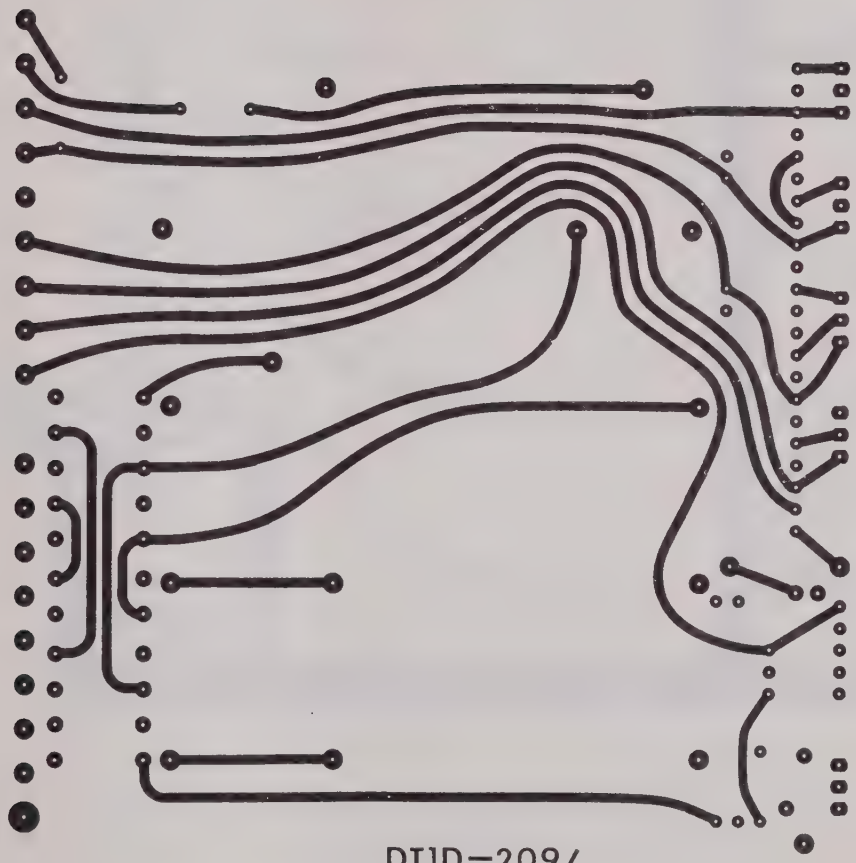

DET IN Receiver Board (A6)
Circuit Pattern
(Non-Component Side)
PMT1D-404

Fig. 5-29



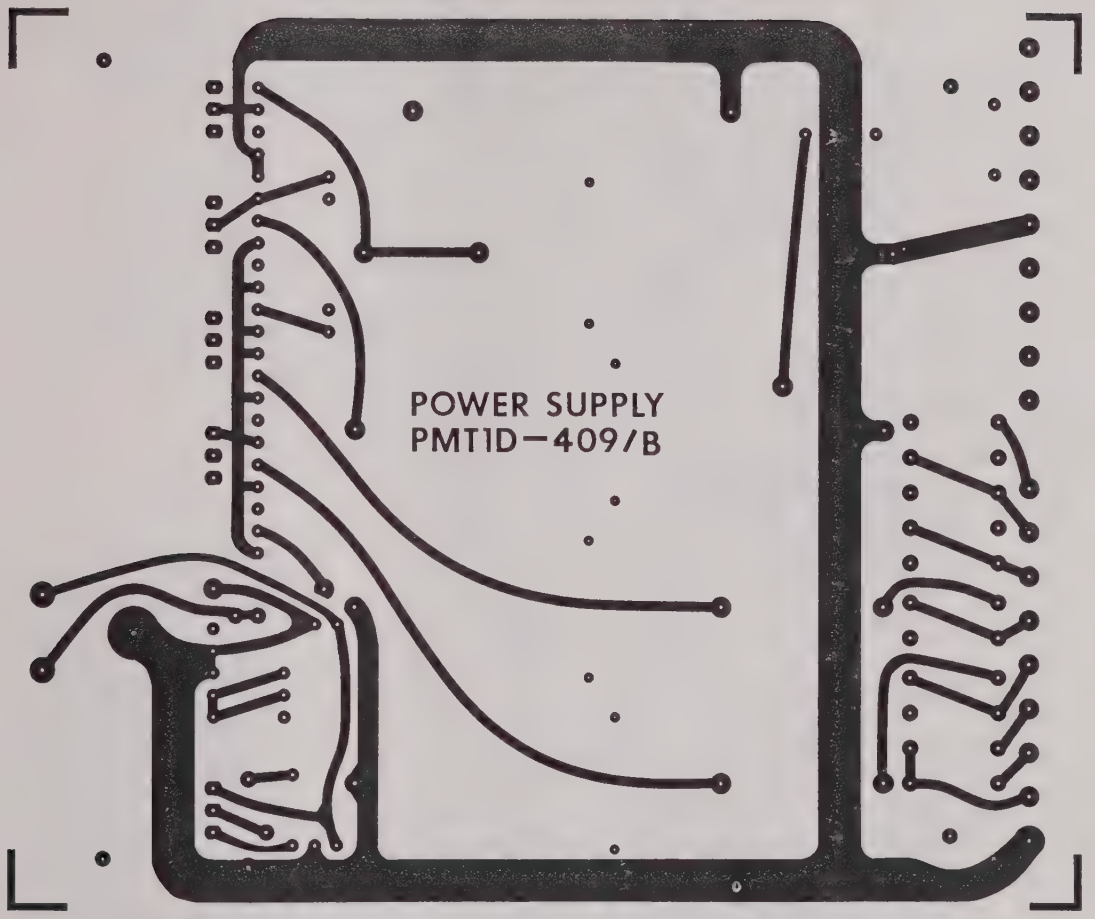

Meter Interface Board (A7)
Circuit Pattern
(Non-Component Side)
PMT1D-407

Fig. 5-30



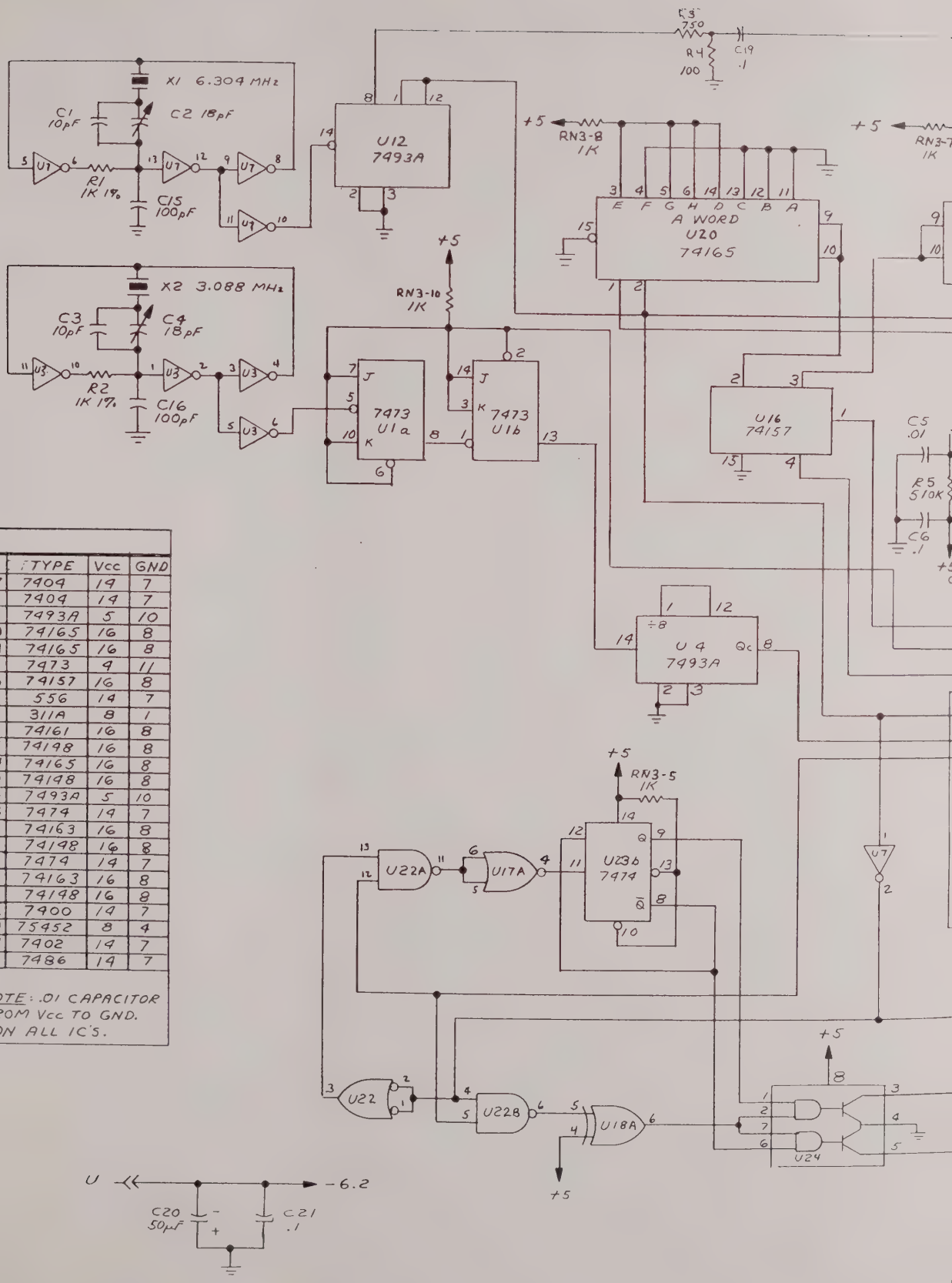

Power Supply Board (A8)
Circuit Pattern
(Component Side)
PMT1D-409

Fig. 5-31



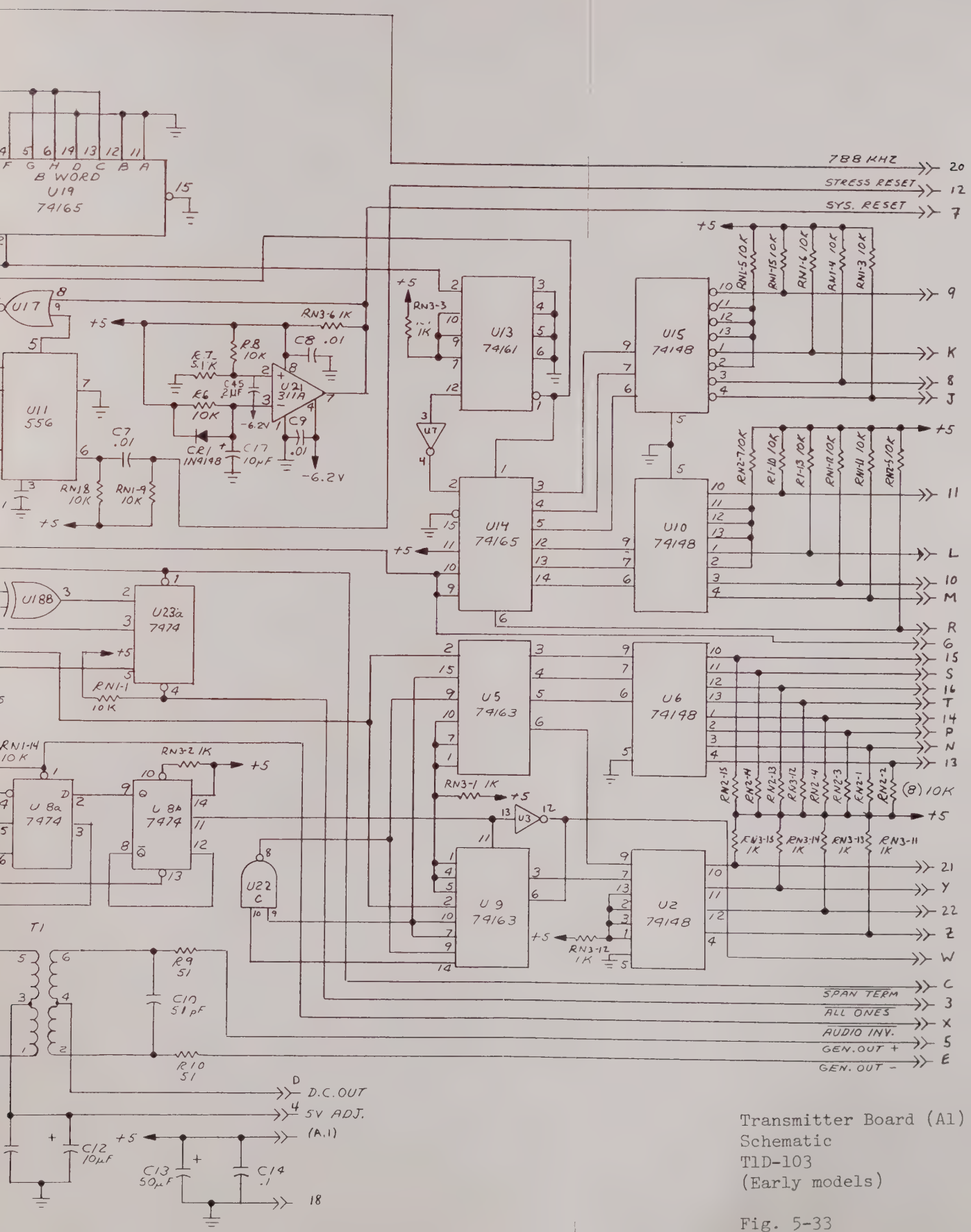

Power Supply Board (A8)
Circuit Pattern
(Non-Component Side)
PMT1D-409

Fig. 5-32




| | TYPE | Vcc | GND |
|---|---|---|---|
| U7 | 7404 | 14 | 7 |
| U3 | 7404 | 14 | 7 |
| U12 | 7493A | 5 | 10 |
| U20 | 74165 | 16 | 8 |
| U19 | 74165 | 16 | 8 |
| U1 | 7473 | 4 | 11 |
| U16 | 74157 | 16 | 8 |
| U11 | 556 | 14 | 7 |
| U21 | 311A | 8 | 1 |
| U13 | 74161 | 16 | 8 |
| U15 | 74198 | 16 | 8 |
| U14 | 74165 | 16 | 8 |
| U10 | 74198 | 16 | 8 |
| U4 | 7493A | 5 | 10 |
| U23 | 7474 | 14 | 7 |
| U5 | 74163 | 16 | 8 |
| U6 | 74198 | 16 | 8 |
| U8 | 7474 | 14 | 7 |
| U9 | 74163 | 16 | 8 |
| U2 | 74198 | 16 | 8 |
| U22 | 7400 | 14 | 7 |
| U24 | 75452 | 8 | 4 |
| U17 | 7402 | 14 | 7 |
| U18 | 7486 | 14 | 7 |

NOTE: .01 CAPACITOR FROM Vcc TO GND. ON ALL IC'S.




Transmitter Board (A1)
Schematic
T1D-103
(Early models)

Fig. 5-33

| REF. DES. | COMPONENT DESCRIPTION | COMPONENT MANUFACTURER | PART NUMBER |
|---|---|---|---|
| **T1D OFFICE REPEATER TEST SET** | | | |
| A5 | Fault Locating Receiver Board Ass'y | Bowmar | T1D-201 |
| A4 | Repeater Interface Board Ass'y | Bowmar | T1D-202 |
| A1 | Transmitter Board Ass'y | Bowmar | T1D-203 |
| A6 | DET IN Receiver Board Ass'y | Bowmar | T1D-204 |
| A2 | Artificial Line Board Ass'y | Bowmar | T1D-205 |
| A3 | T1D/T1C & T1C/T1D Converter Board Ass'y | Bowmar | T1D-206 |
| **FAULT LOCATING RECEIVER** | | | |
| R19,21,23,25,26,79,81, R30,31,R57 - R64,54 | Resistor, 10K, 1/4W, 10% | | RC07GF103J |
| R1,9,43,68,71 | Resistor, 1K, 1/4W, 10% | | RC07GF102J |
| R10 | Resistor, 4.99K, 1/8W, 1% | | RN60C4991F |
| R18, 53 | Resistor, 510, 1/4W, 10% | | RC07GF511J |
| R16,17,20,22,24,32, R33,55,56,69,80,78 | Resistor, 10K, 1/8W, 1% | | RN60C1002F |
| R2, 5 | Resistor, 22.1K, 1/8W, 1% | | RN60C2212F |
| R7 | Resistor, 1K, 1/8W, 1% | | RN60C1001F |
| R11 | Resistor, 866, 1/8W, 1% | | RN60C8660F |
| R28, 29 | Resistor, 715, 1/8W, 1% | | RN60C7150F |
| R3, 4 | Resistor, 10.5K, 1/8W, 1% | | RN60C1052F |
| R8 | Resistor, 1.4K, 1/8W, 1% | | RN60C1401F |
| R27 | Resistor, 576, 1/8W, 1% | | RN55C5760F |
| R52, 49 | Resistor, 324, 1/8W, 1% | | RN55C3240F |
| R47,48,50,51 | Resistor, 2K, 1/8W, 1% | | RN55C2001F |
| R37, 40 | Resistor, 9.26K, 1/8W, 1% | | RN55C9761F |
| R38, 41 | Resistor, 18.2K, 1/8W, 1% | | RN55C1822F |
| R39, 42 | Resistor, 4.32K, 1/8W, 1% | | RN55C4321F |
| R12 | Resistor, 53.6K, 1/8W, 1% | | RN60C5362F |
| R73 | Resistor, 2.26K, 1/8W, 1% | | RN60C2261F |
| R70, 15 | Resistor, 5.1K, 1/4W, 5% | | RC07GF512J |
| R72 | Resistor, 3.92K, 1/4W, 5% | | RN60C3921F |
| R77, 80 | Resistor, 100K, 1/4W, 5% | | RC07GF104J |
| R14 | Resistor, 8.87K, 1/4W, 1% | | RN60C8871F |
| R13 | Resistor, 7.5K, 1/4W, 5% | | RC07GF752J |
| R6 | Resistor, 24.3K, 1/4W, 1% | | RN60C2432F |

| REF. DES. | COMPONENT DESCRIPTION | COMPONENT MANUFACTURER | PART NUMBER |
|---|---|---|---|
| **FAULT LOCATING RECEIVER (Con't)** | | | |
| U4,5,7,9,10,15,20,14 | Integrated Circuit | National Semiconductor | LM301AN |
| U8, 11, 16,6 | Integrated Circuit | Siliconix | DG201CJ |
| U2 | Integrated Circuit | | SN7474N |
| U3 | Integrated Circuit | | SN7404N |
| U12 | Integrated Circuit | National Semiconductor | LM311N |
| U1,13,17,18,19 | Integrated Circuit | Fairchild | UA747PC |
| L1 - L6 | Inductor, 100uh | Lenox-Fugle | NR100 |
| | | | LF100 |
| CR1 - CR10 | Diode | | 1N4148 |
| C25, 26, 58 | Capacitor, .01uf | Centralab | UK-16-103 |
| C2,4-6,8-11,18-22,67-71, C27-30,32,43,45, 34-36, C46,59,61,38,40, 51-57 | Capacitor, .1uf | Sprague | HY850 |
| C24,39,33,37,41,42, C44,48 | Capacitor, 30pf | Sprague | CM04ED300103 |
| C1,3,7, 12-17, 23, C32,47,60 | Capacitor, 10uf, 25V | Mepco/Electra | ET100X025A2 |
| E3 - E8 | Terminals | Cambion | 2027-2 |
| **REPEATER INTERFACE BOARD ASSEMBLY** | | | |
| R1 | Resistor, 33, 1W, 5% | | RC32GF330J |
| R3, 5 | Resistor, 8.87K, 1/8W, 1% | | RN60C8871F |
| R4, 36 | Resistor, 499K, 1/8W, 1% | | RN60C4993F |
| R13 | Resistor, 240K, 1/4W, 5% | | RC07GF2443 |
| R7,8,9,6 | Resistor, 100K, 1/8W, 1% | | RN60C1003F |
| R10 | Resistor, 4.87K, 1/8W, 1% | | RN60C4871F |
| R11 | Resistor, 51.1K, 1/8W, 1% | | RN60C5112F |
| R12,27,32 | Resistor, 10K, 1/4W, 5% | | RC07GF103J |
| R14, 35 | Resistor, 1.2K, 1/4W, 5% | | RC07GF122J |

| REF. DES. | COMPONENT DESCRIPTION | COMPONENT MANUFACTURER | PART NUMBER |
|---|---|---|---|
| REPEATER INTERFACE BOARD ASSEMBLY (Con't) | | | |
| R15 | Resistor, 240, 1/4W, 5% | | RC07GF241J |
| R16 | Resistor, 1M, 1/4W, 5% | | RC07GF105J |
| R17 | Resistor, 750 ohm, 1/4W, 5% | | RC07GF751J |
| R18,19,22,23,28, R31,34,26 | Resistor, 1K, 1/4W, 5% | | RC07GF102J |
| R20, 24 | Resistor, 9.09K, 1/8W, 1% | | RN60C9091F |
| R21, 25, 30 | Resistor, 150, 1/4W, 5% | | RC07GF151J |
| R29 | Resistor, 3K, 1/4W, 5% | | RC07GF302J |
| R33 | Resistor, 22K, 1/4W, 5% | | RC07GF223J |
| R38 | Resistor, 10M, 1/4W, 5% | Mepco/Electra | CR25,PIN5043CX10M-005 or RC07GF106J |
| R37 | Resistor, 4.7, 1/4W, 5% | | RC07GF4R7J |
| C16, 19 | Capacitor, 390pf | | CM04FD391J03 |
| C2,4,6,8 | Capacitor, 50uf, 50V | Sprague | 500D506G050D07 |
| C1,3,5,7,13,14,27, C28,18,21,24 | Capacitor, .01uf, DISC. | Centralab | UK-16-103 |
| C9 | Capacitor, 10uf, 50V | Sprague | 30D106G050CB9 |
| C11,12,17,20,22,25 | Capacitor, .1uf, | Centralab | UK-16-104 |
| C15 | Capacitor, 4.7uf, 10V, 10% | Sprague | 196D475X9010HA1 |
| C23 | Capacitor, 470pf, 5%, SM | CDE | CM04FD471J03 |
| C26 | Capacitor, 10uf, 25V | Sprague | 500D106G025BB7 |
| VR1 | Voltage Regulator | Fairchild | UA7805UC |
| U1, 2 | Integrated Circuit | Fairchild | UA739 |
| U3, 4 | Integrated Circuit | Fairchild | 311 |
| L2 | Inductor Coil, 100uh | Lenox-Fugle | NR-100 |
| Q1 | Transistor | | 2N4091 |
| CR1, CR2 | Diode | | 1N4148 |
| T1,2,3,4, | Transformer | WECO | 2560AL |
| T5 | Transformer | Pulse Engineering | PE-5763 |

| REF. DES. | COMPONENT DESCRIPTION | COMPONENT MANUFACTURER | PART NUMBER |
|---|---|---|---|
| **TRANSMITTER** | | | |
| X1 | Crystal, 6.304 MHz | Bowmar | B6441 |
| X2 | Crystal, 3.088 MHz | Bowmar | B6440 |
| R11 | Resistor, 330, 1/4W, 5% | | RC07GF331J |
| R1, 2 | Resistor, 3.92K, 1/8W, 1% | | RN60C3921F |
| RN3 | Resistor, 1K, Array | Beckman | 898-1-R1K |
| R5 | Resistor, 510K, 1/4W, 5% | | RC07GF514J |
| R6, 8 | Resistor, 10K, 1/4W, 5% | | RC07GF103J |
| R7 | Resistor, 5.1K, 1/4W, 5% | | RC07GF512J |
| R9, 10 | Resistor, 51, 1/4W, 5% | | RC07GF510J |
| RN1, RN2 | Resistor, 10K, Array | Beckman | 898-1-R10K |
| R3 | Resistor, 750, 1/4W, 5% | | RC07GF751J |
| R4 | Resistor, 100 | | RC07GF101J |
| R12, 13 | Resistor, 1K, 1/4W, 1% | | RN55C1001F |
| C1 | Capacitor, 18pf, 5% | Sprague | 561CP3KBA102AE180J |
| C2, 4 | Capacitor, Variable, 1-18pf | Erie | 567-013 |
| C45 | Capacitor, .2uf, DISC | Centralab | UK-16-204 |
| C7,8,9,C22-44 | Capacitor, .01uf, DISC | Centralab | UK-16-103 |
| C5 | Capacitor, .33uf, 20%, 50V | | 8131-050-651-334M |
| C6,11,14,18,19,21 | Capacitor, .1uf, DISC | Centralab | UK-16-104 |
| C12, 17 | Capacitor, 10uf, 25V | Sprague | 500D106G025BB5 |
| C13 20 | Capacitor, 50uf, 50V | Sprague | 500D506G050DD5 |
| C15, 16 | Capacitor, 1000pf, 5% | CDE | CM06FD102J03 |
| CR1 | Diode | | 1N4148 |
| C46 | Capacitor, S. Mica, 100pf | | CM04FD101J03 |
| U3, U7 | Integrated Circuit | | 74LS04N |
| U4, 12 | Integrated Circuit | | SN7493AN |
| U20,19,14 | Integrated Circuit | | SN74165N |
| U1 | Integrated Circuit | | SN7473N |
| U16 | Integrated Circuit | | SN74157N |
| U11 | Integrated Circuit | | NE556N |
| U21 | Integrated Circuit | | LM311AN |
| U13 | Integrated Circuit | | SN74161N |
| C3 | Capacitor, 30pf | Sprague | 561CP3KBA102AE300J |

| REF. DES. | COMPONENT DESCRIPTION | COMPONENT MANUFACTURER | PART NUMBER |
|---|---|---|---|
| **TRANSMITTER (Con't)** | | | |
| U2,10,6,15 | Integrated Circuit | | SN74148N |
| U8, 23 | Integrated Circuit | | SN7474N |
| U5, 9 | Integrated Circuit | | SN74163N |
| U22 | Integrated Circuit | | SN7400N |
| U24 | Integrated Circuit | | SN75452BD |
| U17 | Integrated Circuit | | SN7402N |
| U18 | Integrated Circuit | | SN7486N |
| T1 | Transformer | Pulse Engineering or AIE | PE-8272 or 318-0466 |
| **DETECTOR IN RECEIVER** | | | |
| R1, 41 | Resistor, 10, 1/4W, 5% | | RC07GF100J |
| R2,22,11,14,21,34, R39,42,45,40,48 | Resistor, 1K, 1/4W, 5% | | RC07GF102J |
| R19 | Resistor, 240, 1/4W, 5% | | RC07GF241J |
| R4,9,10 | Resistor, 5.1K, 1/4W, 5% | | RC07GF512J |
| R6,8,38 | Resistor, 2K, 1/4W, 5% | | RC07GF202J |
| R7 | Resistor, 2.2K, 1/4W, 5% | | RC07GF222J |
| R12, 20 | Resistor, 100, 1/4W, 5% | | RC07GF101J |
| R17 | Resistor, 750, 1/4W, 5% | | RC07GF751J |
| R18 | Resistor, 1M, 1/4W, 5% | | RC07GF105J |
| R15 | Resistor, 13K, 1/4W, 5% | | RC07GF133J |
| R16 | Resistor, 11.8K, 1/8W, 1% | | RN60C1182F |
| R13 | Resistor, 2K, 1/8W, 1% | | RN60C2001F |
| R3 | Resistor, 1.07K, 1/8W, 1% | | RN60C1071F |
| R23,24,29,30,32 | Resistor, 10K, 1/4W, 5% | | RC07GF103J |
| R25, 31 | Resistor, 100K, 1/4W, 5% | | RC07GF104J |
| R26, 33 | Resistor, 300, 1/4W, 5% | | RC07GF301J |
| R28 | Resistor, 8.2K, 1/4W, 5% | | RC07GF822J |
| R35 | Resistor, 200, 1/4W, 5% | | RC07GF201J |
| R36 | Resistor, 240, 1/4W, 5% | | RC07GF241J |
| R37 | Resistor, 470, 1/4W, 5% | | RC07GF471J |
| R43 | Resistor, 23.7K, 1/8W, 1% | | RN60C2372F |
| R44 | Resistor, 6.81K, 1/8W, 1% | | RN60C6811F |
| R27,45,5 | Resistor, 15K, 1/4W, 5% | | RC07GF153J |
| R49 | Resistor, 50, 1/4W, 5% | | RC07GF500J |

| REF. DES. | COMPONENT DESCRIPTION | COMPONENT MANUFACTURER | PART NUMBER |
|---|---|---|---|
| DETECTOR IN RECEIVER (Con't) | | | |
| E1 - E4 | Standoffs | Cambion | 2027-2 |
| C1,2,6,8,12,35,9,25, C24,30,33,37 | Capacitor, .1uf, DISC | Centralab | UK-16-104 |
| C3,4,10,11 | Capacitor, 51pf, 5%, SM | CDE | CM04FD510J03 |
| C5,13,14 | Capacitor, 4.7uf, 35V, 10% | Sprague | 196D475X903S5A1 |
| C7,17,23,20, 39-49 | Capacitor, .01uf | Centralab | UL-16-103 |
| C15 | Capacitor, 100pf, 5%, SM | CDE | CM04CD101J03 |
| C16, 22 | Capacitor, 1uf, 50V | Sprague | 500D105G050BA7 |
| C24,26,21 | Capacitor, 20pf, 5%, SM | CDE | CM04CD200J03 |
| C27 | Capacitor, 1-18pf | Erie | 567-013 |
| C28 | Capacitor, 12pf, 5%, SM | CDE | CM04CD120J03 |
| C31 | Capacitor, 3900pf, 5%, SM | CDE | CM06CD392J03 |
| C32 | Capacitor, 47uf, 6V | Sprague | 150D476X901DR2 |
| C34,36,38 | Capacitor, 50uf, 50V | Sprague | 500D506G050DD7 |
| C18, 19 | Capacitor, 30pf, 5%, SM | CDE | CM04CD300J03 |
| L1,3,4,5,6,7 | Inductor Coil, 100uh | Lenox Fugle | NR100 |
| L2 | Inductor Coil, 39uh, | Bowmar | B6346 |
| T1 | Transformer | Pulse Engineering | PE-5763 |
| T2 | Transformer | Pulse Engineering | PE5763 |
| U1, U4 | Integrated Circuit | | 75107A |
| U2 | Integrated Circuit | | CA3083 |
| U7 | Integrated Circuit | | 7404N |
| U8 | Integrated Circuit | | 7400N |
| U11, 13 | Integrated Circuit | | 7474N |
| U9, 5 | Integrated Circuit | | 7473N |
| U10 | Integrated Circuit | | 556N |
| U3,14,12 | Integrated Circuit | | 74123N |
| U6 | Integrated Circuit | | 7402N |
| CR1 | Diode | | 1N4148 |
| Q1, 2 | Transistor | | 2N2369A |
| Q3 | Transistor | | 2N4091 |
| Q4,5,6,7,8 | Transistor | | 2N3904 |

| REF. DES. | COMPONENT DESCRIPTION | COMPONENT MANUFACTURER | PART NUMBER |
|---|---|---|---|
| **ARTIFICIAL LINE BOARD ASSEMBLY** | | | |
| C1, 6 | Capacitor, 6490pf | | KS-16742, L32 |
| C2 | Capacitor, 3650pf | | KS-16742, L32 |
| C3 | Capacitor, 2430pf | | KS-16742, L32 |
| C4 | Capacitor, 2370pf | | KS-16742, L32 |
| C5 | Capacitor, 10,000pf | | KS-16742, L32 |
| L8, 10 | Inductor, 33uh | | KS-13726, L24 |
| L3,5,7,9 | Inductor, 12uh | | KS-13726, L62 |
| L4, 6 | Inductor, 18uh | | KS-13726, L64 |
| L1, 2 | Inductor, 82uh | | KS-13726, L47 |
| R19, 31 | Resistor, 24.3 | | KS-20810, L1A |
| R2,3,5,6,10, 13-15, R20 - 23, R26-29 | Resistor, 49.9 | | KS-20810, L1A |
| R25 | Resistor, 182 | | KS-20810, L1A |
| R9, 17 | Resistor, 13 | | KS-20810, L1A |
| R11 | Resistor, 271 | | KS-20810, L1A |
| R12 | Resistor, 383 | | KS-20810, L1A |
| R16, 8 | Resistor, 18.7 | | KS-20810, L1A |
| R18, 30 | Resistor, 12.1 | | KS-20810, L1A |
| R1, 7 | Resistor, 33.2 | | KS-20810, L1A |
| R24 | Resistor, 340 | | KS-20810, L1A |
| R4 | Resistor, 121 | | KS-20810, L1A |
| **T1D/T1C & T1C/T1D CONVERTER BOARD ASSEMBLY** | | | |
| C1 | Capacitor, .022uf | | KS-19774, L6 |
| C2,3,5,6,11,26,27, C32,44,46,47 | Capacitor, 1uf | Western Electric | 650B |
| C7,4,16,17, 20-22, C25, 29 | Capacitor, 33uf | Western Electric | 651D |
| C9 | Capacitor, 1.5pf | | KS-20676, L17 |
| C10 | Capacitor, 4.42pf | | KS-14115, L19 |
| C12 | Capacitor, 75pf | | KS-20676, L1 |
| C13 | Capacitor, 712pf | | KS-20676, L3 |

| REF. DES. | COMPONENT DESCRIPTION | COMPONENT MANUFACTURER | PART NUMBER |
|---|---|---|---|
| T1D/T1C & T1C/T1D CONVERTER BOARD ASSEMBLY (Con't) | | | |
| C14 | Capacitor, 475pf | | KS-20676, L3 |
| C15 | Capacitor, 1100pf | | KS-20676, L1 |
| C18,31,33,34,36, C37,41,23,24 | Capacitor, .1uf | Western Electric | 743G |
| C19,45,28 | Capacitor, .01uf | Western Electric | 743G |
| C30 | Capacitor, 3.74pf | | KS-14115, L19 |
| C42 | Capacitor, 2pf | | KS-16958, L27 |
| C43 | Capacitor, .22uf | | KS-19774, L5 |
| C48 | Capacitor, 10pf | | KS-16958, L27 |
| Y1, 2 | Crystal | Western Electric | 117AAC |
| CR1 | Diode | Western Electric | 533F |
| CR2, 3 | Diode | Western Electric | 808CE |
| CR4 | Diode | Western Electric | 458C |
| L1 | Inductor, 84uh | | KS-19680, L43 |
| L2 | Inductor, 76uh | | KS-20927, L70 |
| L3 | Inductor, 22uh | | KS-19680, L3 |
| L4 | Inductor, 130uh | | KS-19680, L36 |
| L5 | Inductor, 143uh | | KS-19680, L61 |
| L6, 7 | Inductor, 12uh | | KS-19680, L62 |
| L8 | Inductor, 8.2uh | | KS-20927, L64 |
| L9 | Inductor, 82uh | | KS-19680, L55 |
| T1, 2 | Transformer | Western Electric | 2662E |
| T3 | Transformer | Western Electric | 2661F |
| T4 | Transformer | Western Electric | 2667K |
| IC1 | Integrated Circuit | Western Electric | 684B (TED) |
| IC2 | Integrated Circuit | Western Electric | 605U (TED) |
| IC3 | Integrated Circuit | Western Electric | 502EK |
| IC4, 5 | Integrated Circuit | Western Electric | 129CS |
| IC6 | Integrated Circuit | Western Electric | 502BK |
| IC7 | Integrated Circuit | Western Electric | 502HG |
| IC8 | Integrated Circuit | Western Electric | 502HF |
| E1-4, 7,8, 13-19, E21,22, 23,26,29, E30,31 | Terminals | Cambion | 140-1785-02-01-00 |

| REF. DES. | COMPONENT DESCRIPTION | COMPONENT MANUFACTURER | PART NUMBER |
|---|---|---|---|
| **T1D/T1C & T1C/T1D CONVERTER BOARD ASSEMBLY (Con't)** | | | |
| R10, 67 | Potentiometer, 100 ohm | | KS-19055, L3 |
| R12 | Potentiometer, 5K | | KS-19055, L3 |
| R14 | Potentiometer, 1K | | KS-19055, L3 |
| R1 | Resistor, 140 | | KS-20616, L1A |
| R2 | Resistor, 121 | | KS-20616, L1A |
| R3 | Resistor, 1330 | | KS-20616, L1A |
| R4,5,6,7 | Resistor, 402 | | KS-20616, L1A |
| R8 | Resistor, 379 | | KS-20616, L1A |
| R9 | Resistor, 110 | | KS-20616, L1A |
| R11 | Resistor, 562 | | KS-20616, L1A |
| R13, 68 | Resistor, 100 | | KS-20616, L1A |
| R15,23,29,48,49,52 | Resistor, 10 | | KS-20616, L1A |
| R16,17,33,35,45 | Resistor, 4.99K | | KS-20616, L1A |
| R18 | Resistor, 2.8K | | KS-20616, L1A |
| R19 | Resistor, 90.9 | | KS-20616, L1A |
| R20 | Resistor, 2K | | KS-20616, L1A |
| R21 | Resistor, 47 | | KS-20616, L1A |
| R22 | Resistor, 383 | | KS-20616, L1A |
| R24 | Resistor, 499 | | KS-20616, L1A |
| R25 | Resistor, 20 | | KS-20616, L1A |
| R26,31,47 | Resistor, 5620 | | KS-20616, L1A |
| R27 | Resistor, 5990 | | KS-20616, L1A |
| R28 | Resistor, 487 | | KS-20616, L1A |
| R32, 34 | Resistor, 2520 | | KS-20616, L1A |
| R37 | Resistor, 1100 | | KS-20616, L1A |
| R36 | Resistor, 619 | | KS-20616, L1A |
| R38 | Resistor, 301 | | KS-20616, L1A |
| R39, 40 | Resistor, 1 | | KS-20616, L1A |
| R41, 42 | Resistor, 5.62 | | KS-20616, L1A |
| R43 | Resistor, 1800 | | KS-20616, L1A |
| R44, 51 | Resistor, 30.1 | | KS-20616, L1A |
| R46, 30 | Resistor, 1430 | | KS-20616, L1A |

| REF. DES. | COMPONENT DESCRIPTION | COMPONENT MANUFACTURER | PART NUMBER |
|---|---|---|---|
| **T1D/T1C & T1C/T1D CONVERTER BOARD ASSEMBLY (Con't)** | | | |
| R50 | Resistor, 750 | | KS-20616, L1A |
| R55, 58 | Resistor, 15K | | KS-20616, L1A |
| R59 | Resistor, 7.5K | | KS-20616, L1A |
| R56, 57 | Resistor, 8.45K | | KS-20616, L1A |
| R60 | Resistor, 2490 | | KS-20616, L1A |
| R61, 62 | Resistor, 2050 | | KS-20616, L1A |
| R69 | Resistor, 10K | | KS-20616, L1A |
| R71, 72 | Resistor, 301 | | KS-20616, L1A |
| R70, 73 | Resistor, 37.4 | | KS-20616, L1A |
| **METER BOARD ASSEMBLY** | | | |
| R1 | Resistor, 10K, 1/4W, 1% | | RN55C Type |
| R2 | Resistor, 4.7K, 1/4W, 5% | | RC07 Type |
| C1, 2 | Capacitor, .1uf | Unitrode | CGD104ZDZ |
| C3 | Capacitor, 680uf, 25V | Mepco/Electra | ET681X0225A02 |
| U1 | Integrated Circuit | | 741RC |
| T1 | Transformer | AIE | 95-0207 |
| **POWER SUPPLY ASSEMBLY** | | | |
| VR1 | +15 VDC Reg. W/Mica Insulator & Shoulder Washer | Fairchild | UA7815UC |
| VR2 | +6 VDC Reg. W/Mica Insulator & Shoulder Washer | Fairchild | UA7806UC |
| VR3 | -6 VDC Reg. W/Mica Insulator & Shoulder Washer | Fairchild | UA7906UC |
| VR4 | -15 VDC Reg. W/Mica Insulator & Shoulder Washer | Fairchild | UA7915UC |
| VR5 | +5 VDC Reg. W/Mica Insulator & Shoulder Washer | Fairchild | UA7805KC |
| VR6 | 5 VDC Reg. W/Mica Insulator & Shoulder Washer | Fairchild | UA7805UC |

| REF. DES. | COMPONENT DESCRIPTION | COMPONENT MANUFACTURER | PART NUMBER |
|---|---|---|---|
| **POWER SUPPLY ASSEMBLY (Con't)** | | | |
| CR1 | Diode | | 1N4002 |
| CR2 - CR11 | Diode | | 1N4001 |
| CR12 | Diode, Zener | | 1N5908 |
| R1, 4 | Resistor, 240, 1/4W, 5% | | RC07GF241J |
| R2, 3 | Resistor, 6.2, 1/4W, 5% or 1/2W, 5% or 2% | RLR20C6R2J or RLR20C6R2G or | RC07GF6R2J |
| R5 | Resistor, 2K, 1/4W, 5% | | RC07GF202J |
| R8 | Resistor, 1K, 1/4W, 5% | | RC07GF102J |
| R6 | Potentiometer, 500 | Beckman | 89WR500 |
| R7 | Resistor, 1M, 1/4W, 5% | | RC07GF105J |
| C1 | Capacitor, 35uf, 150V | Sprague | 500D356F150FH7 |
| C2,3,4,5 | Capacitor, 2500uf, 50V | Mepco/Electra | 3050HP252U050 |
| C6,7,8,12,14,16 | Capacitor, .33uf | Sprague | 196D334X9035HA1 |
| C9,10,11,13,15,17 | Capacitor, 1uf | Sprague | 196D155X9025HA1 |
| E1 - 18 | Terminals | Cambion | 2027-2 |
| CR14,15,16 | Diode | | 1N4148 |
| **FRONT PANEL ASSEMBLY** | | | |
| M1 | Meter | Bowmar | A-T1D-012 |
| XF1 | 3AG Fuse Extractor Post | Littlefuse | 342004 |
| F1 | 3AG Slo-Blo Fuse, 1/2A | Littlefuse | 313500 |
| J1,3,4 | Phone Jack | Switchcraft | MT333B |
| XDS1 | Lamp, Midget Screw 6V | Chicago Miniature | 1768 |
| S8 | Switch, Rocker, Illum. SPDT | C & K | 5101 |
| S6 | Switch, Slide, DPTT | Switchcraft | 46313LDR |
| S11 | Switch, Slide, DPDT | Stackpole | S-9022C003-0 |
| S3 | Pushbutton, Mon, DPDT | C & K | 8121 |
| S1 | Filter Switch Assembly | Bowmar | LM-T1D-221 |
| S2 | Stress Density Switch Assembly | Bowmar | LM-T1D-222 |

| REF. DES. | COMPONENT DESCRIPTION | COMPONENT MANUFACTURER | PART NUMBER |
|---|---|---|---|
| **FRONT PANEL ASSEMBLY (Con't)** | | | |
| S4 | Art Line Switch Assembly | Bowmar | LM-T1D-223 |
| S5 | Repeater Power Switch Assembly | Bowmar | LM-T1D-224 |
| S9 | Repeater Test Switch Assembly | Bowmar | LM-T1D-225 |
| S10 | Function Switch Assembly | Bowmar | LM-T1D-226 |
| S7/R1 | Receiver Sensitivity Switch Assembly | Bowmar | LM-T1D-227 |
| DS2 - DS6 | LED, Red with Clip & Repeater Ring | Hewlett Packard | 5082-4650 |
| R2 | Potentiometer | Clarostat | RV4NAYSD251A |
| R3 | Potentiometer | Clarostat | RV6NAYSD102A |
| R4, 5 | Resistor, 458, 1/10W, 1% | | RN55C4580F |
| R6 | Resistor, 910, 1/4W, 5% | | RC07GF911J |
| J2, 5 | Phone Jack | Switchcraft | MT334B |
| **S1 - FILTER SWITCH ASSEMBLY** | | | |
| S1 | Switch, Rotary, 2 Pole, 2 Deck | Centralab | PA-2004 |
| **S2 - STRESS DENSITY SWITCH ASSEMBLY** | | | |
| S2 | Switch, Rotary, 5 Pole, 5 Deck | Centralab | PA-1017 |
| R1 | Resistor, 1.50K, 1/4W, 1% | | RN55 |
| R2, 4 | Resistor, 1.58K, 1/4W, 1% | | RN55 |
| R3 | Resistor, 1.65K, 1/4W, 1% | | RN55 |
| R5 | Resistor, 1.37K, 1/4W, 1% | | RN55 |
| **S4 - ART LINE SWITCH ASSEMBLY** | | | |
| S4 | Switch, Rotary, 6 Pole, 2 Deck | Centralab | PA-1019 |
| **S5 - REPEATER TEST SWITCH ASSEMBLY** | | | |
| S5 | Index Assembly | Centralab | PA-301 |
| R1, 2, 3 | Resistor, 100, 1/10W, 1% | | RN55C1001F |

| REF. DES. | COMPONENT DESCRIPTION | COMPONENT MANUFACTURER | PART NUMBER |
|---|---|---|---|
| **S9 - REPEATER POWER SWITCH ASSEMBLY** | | | |
| S9 | Switch, Rotary, 2 Pole, 1 Deck | Centralab | PA-1003 |
| **S10 - FUNCTION SWITCH ASSEMBLY** | | | |
| S10 | Switch, Rotary, 6 Pole, 6 Deck | Centralab | PA-1023 |
| CR1, 2 | Diode | | 1N4148 |
| R1 | Resistor, 100, 1/10W, 1% | | RN55C1000F |
| R2 | Resistor, 240, 1/4W, 5% | | RC07GF241J |
| **S7/R1 RECEIVER SENSITIVITY SWITCH ASSEMBLY** | | | |
| S7/R1 | Switch, Rotary, 4 Deck, 1 Pole per Deck with 10K Pot. | Centralab | PA0570-0013 |
| R7, 8 | Resistor, 1.18K, 1/10W, 1% | | RN55C1181 |
| R2,3,5,6 | Resistor, 1.24K, 1/10W, 1% | | RN55C1241 |
| R4 | Resistor, 1.74K, 1/10W, 1% | | RN55C1741 |



NOTE: Metal film resistors may be substituted for carbon composition resistors as follows:

RLR07C for RC07
RLR20C for RC20
RLR32C for RC32